Compact Dual-Phase Synchronous-Rectified Buck Controller

General Description

The uP1605 is a compact dual-phase synchronous-rectified Buck controller specifically designed to deliver high quality output voltage for high power applications. This part is capable of delivering up to 60A output current thanks to its embedded bootstrapped drivers that support 12V + 12V driving capability. The uP1605 features configurable gate driving voltage for maximum efficiency and optimal performance. The built-in bootstrap diode simplifies the circuit design and reduces external part count and PCB space.

The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The uP1605 adopts DCR current sensing technique for over current protection and droop control. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to VQFN4x4-24L package.

Ordering Information

Order Number	Package Type	Top Marking
uP1605PQAG	VQFN4x4-24L	uP1605P
uP1605QQAG		uP1605Q
uP1605P: V_{BOOT} = 1.2V uP1605Q: V_{BOOT} = 0.9V		

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

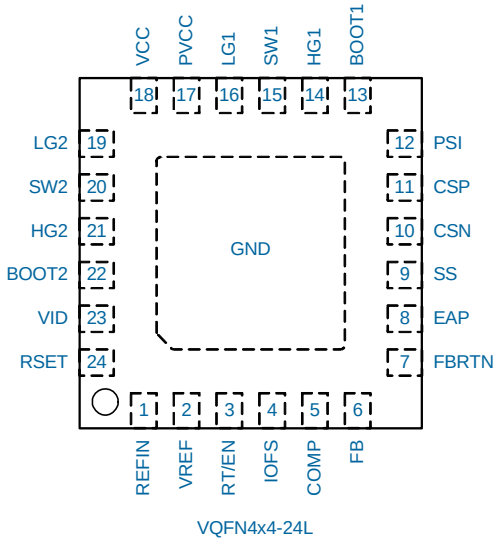
Features

- **Operate with Single Supply Voltage**
- **±2.0% Over Line Voltage and Temperature**
- **Simple Single-Loop Voltage-Mode Control**
- **12V Bootstrapped Drivers with Internal Bootstrap Diode**
- **Adjustable Over Current Protection by DCR Current Sensing**
- **Adjustable Current Balancing by $R_{DS(ON)}$ Current Sensing**
- **Adjustable Operation Frequency form 50kHz to 1MHz Per Phase**
- **External Compensation**
- **Dynamic Output Voltage Adjustment**
- **Adjustable Soft Start**
- **VQFN4x4-24L Package**
- **RoHS Compliant and Halogen Free**

Applications

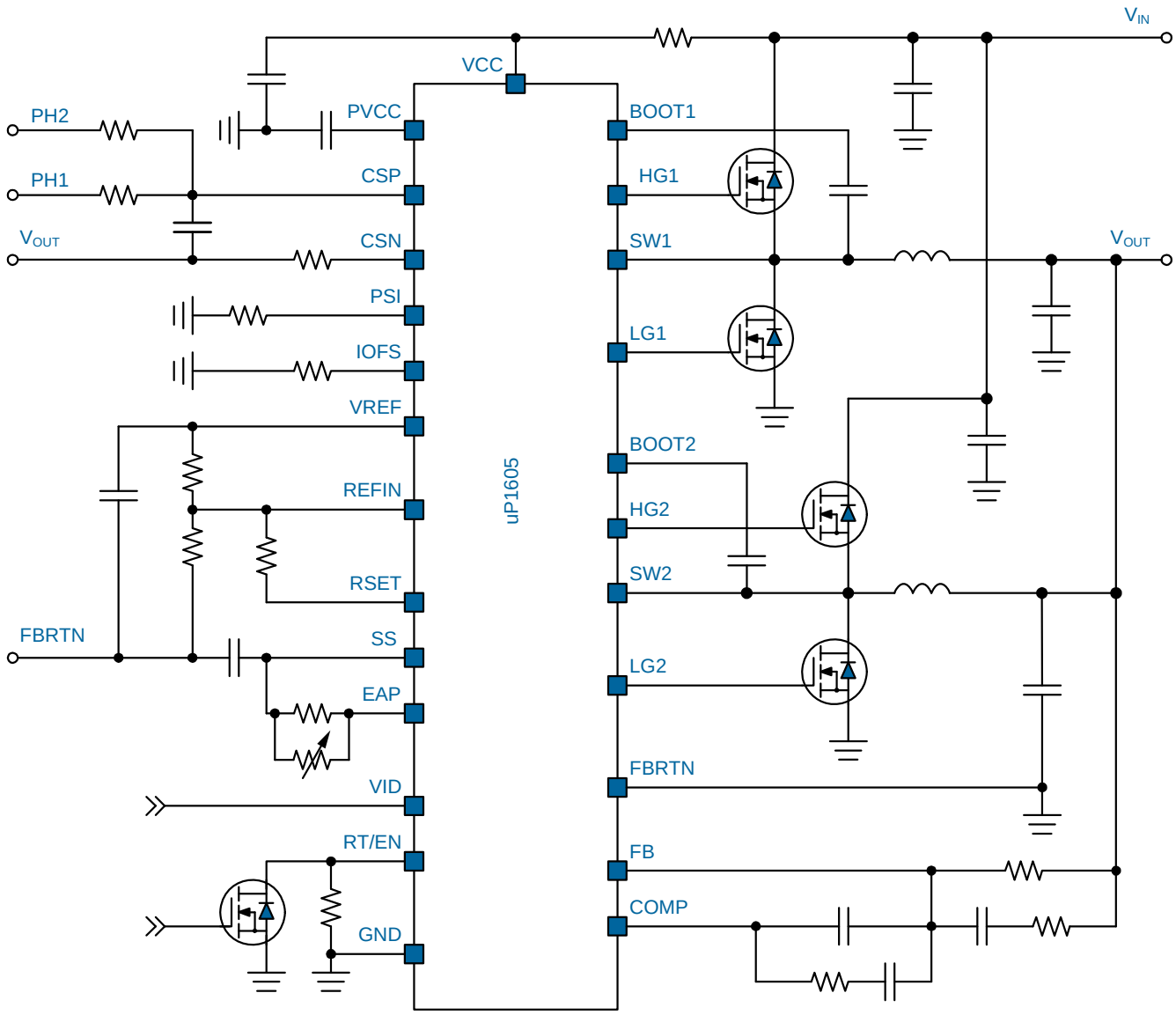
- **Middle-High End GPU Core Power**
- **High End Desktop PC Memory Core Power**
- **Low Output Voltage, High Power Density DC-DC Converters**
- **Voltage Regulator Modules**

Pin Configuration



VQFN4x4-24L

Typical Application Circuit



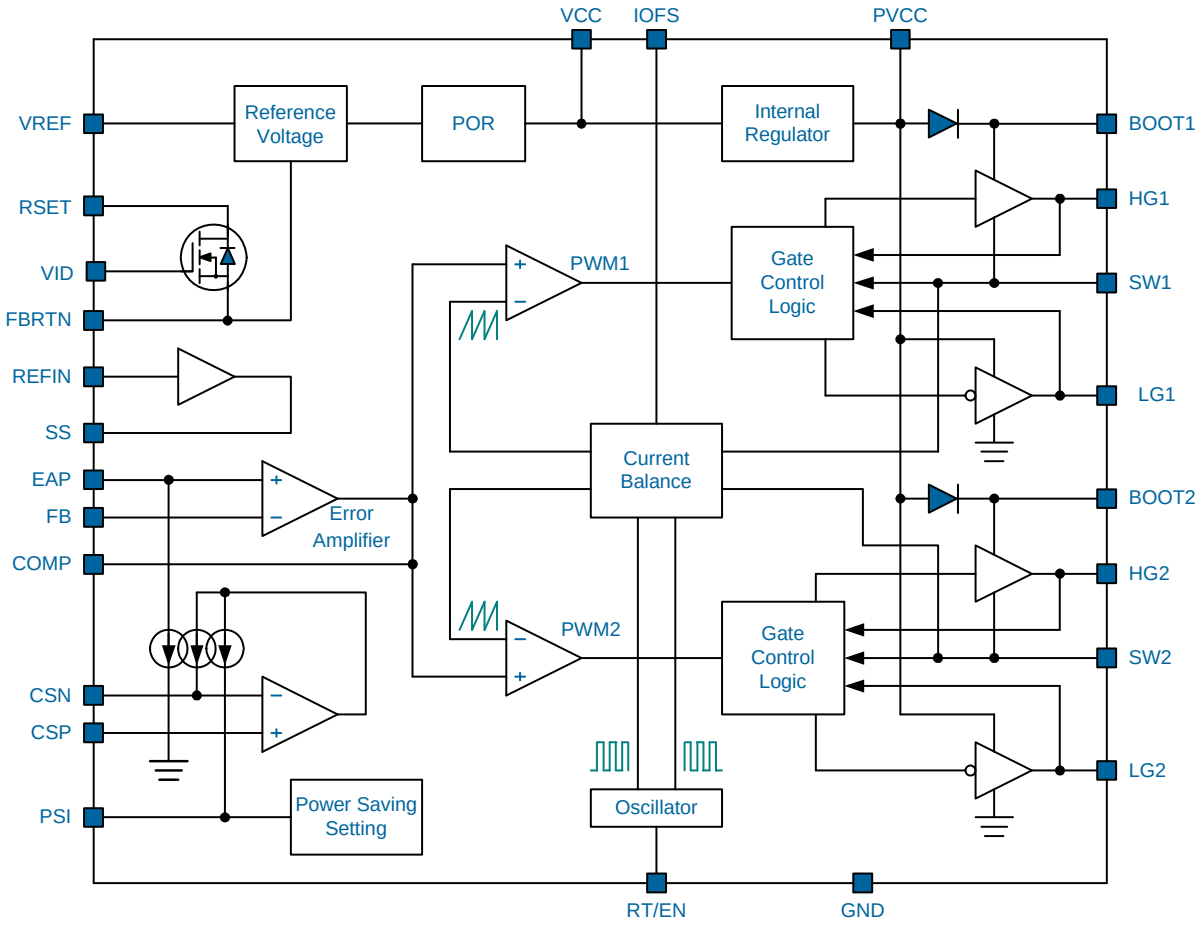
Functional Pin Description

No.	Pin Name	Pin Function
1	REFIN	**External Reference Input.** This is input pin of external reference voltage. Connect a voltage divider from VREF to REFIN to FBRTN to set the reference voltage.
2	VREF	**Output for Reference Voltage.** This is the output pin of high precision 2V reference voltage. Bypass this pin with a 1uF ceramic capacitor to FBRTN.
3	RT/EN	**Operation Frequency Setting.** Connecting a resistor between this pin and GND to set the operation frequency. Pull this pin to ground to shut down the uP1605.
4	IOFS	**Current Balance Adjustment.** Connect a resistor from this pin to VREF or GND to adjust the current sharing.
5	COMP	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
6	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. Use this pin in combination with the COMP pin to compensate the voltage control feedback loop of the converter.
7	FBRTN	**Feedback Return.** Connect this pin to the ground pin where the output voltage is to be regulated.
8	EAP	**Non-Inverting Input of Error Amplifier.** Connect a resistor to SS pin to set the droop slope.
9	SS	**Soft Start Output.** Connect a capacitor to FBRTN to set the soft start interval.
10	CSN	**Negative Input for Current Sensing Amplifier.**
11	CSP	**Positive Input for Current Sensing Amplifier.**
12	PSI	**Power Saving Mode.** Connect a resistor from PSI to GND to set the power saving mode threshold current level. Connect this pin to VREF for always two phase operation. Short this pin to ground for always single phase operation.
13	BOOT1	**Bootstrap Supply** for the floating upper gate driver of channel 1. Connect the bootstrap capacitor C_{BOOT} between BOOT1 pin and the SW1 pin to form a bootstrap circuit.
14	HG1	**Upper Gate Driver Output for Channel 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
15	SW1	**Switch Node for Channel 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
16	LG1	**Lower Gate Driver Output for Channel 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
17	PVCC	**Supply Voltage for Gate Driver.** This pin is the output of internal 9V LDO for providing bias current for internal gate drivers. Connect PVCC to VCC directly to bypass the LDO and operate the gate drivers with 12V supply voltage. A minimum 1uF ceramic capacitor is required for locally filtering the PVCC.
18	VCC	**Supply Voltage.** This pin provides current for internal control circuit and 9V LDO. Bypass this pin with a minimum 1uF ceramic capacitor next to the IC.

Functional Pin Description

No.	Pin Name	Pin Function
19	LG2	**Lower Gate Driver Output for Channel 2.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
20	SW2	**Switch Node for Channel 2.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the HG2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
21	HG2	**Upper Gate Driver Output for Channel 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
22	BOOT2	**Bootstrap Supply** for the floating upper gate driver of channel 2. Connect the bootstrap capacitor C_{BOOT} between BOOT2 pin and the SW2 pin to form a bootstrap circuit.
23	VID	**VID Input.** This pin is used to adjust reference voltage. Logic high turns on the internal MOSFET connected to RSET pin.
24	RSET	**Reference Voltage Setting.** This pin is an open drain output that is pulled low when VID = high. Connect a resistor from this pin to REFIN pin to set the reference voltage.
Exposed Pad GND		**Power Ground.** Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Block Diagram



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The output voltage is precisely regulated to the reference input that is dynamically adjustable by external voltage divider. The uP1605 adopts DCR current sensing technique for over current protection and droop control. The adjustable current balance is achieved by $R_{DS(ON)}$ current sensing technique.

This part features comprehensive protection functions including over current protection, input/output under voltage protection, over voltage protection and over temperature protection.

Other features include adjustable soft start, adjustable operation frequency, and quick response to step load transient. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part comes to VQFN4x4-24L package.

Power On Reset and Initialization

The uP1605 works with a single supply voltage at VCC pin. The VCC voltage is continuously monitored for power on reset (POR) to ensure the supply voltage is high enough for normal operation of the device. The POR threshold level is typically 9V at VCC rising.

9V LDO for Gate Drivers

The uP1605 provides flexible gate driving voltage for maximum efficiency and optimal performance. It integrates two linear regulators providing optimal supply voltages for gate drivers and control circuitry as shown in Figure 1. The 9V linear regulator generates 9V PVCC for gate drives achieving optimum balance efficiency and thermal management. 9V driving voltage reduces the power dissipation at uP1605 to an acceptable level at large gate capacitance and high switching frequency applications. A minimum 1uF ceramic capacitor is required for locally bypassing the PVCC pin. Place the bypass capacitors physically near the IC.

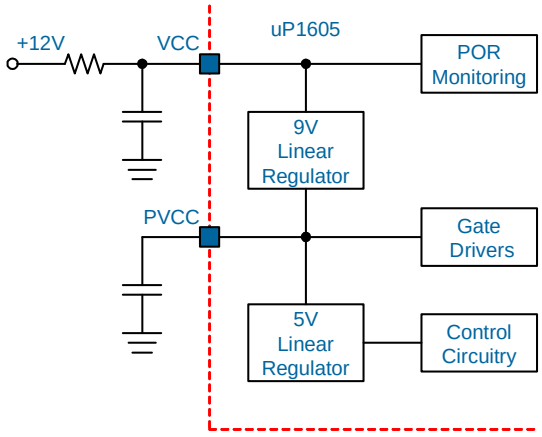


Figure 1. Supply Voltage Configuration for 9V Driving.

The PVCC pin can be tied to VCC pin as shown in Figure 2. This bypasses the 9V LDO and operates the gate drivers with 12V voltage, providing maximum converter efficiency.

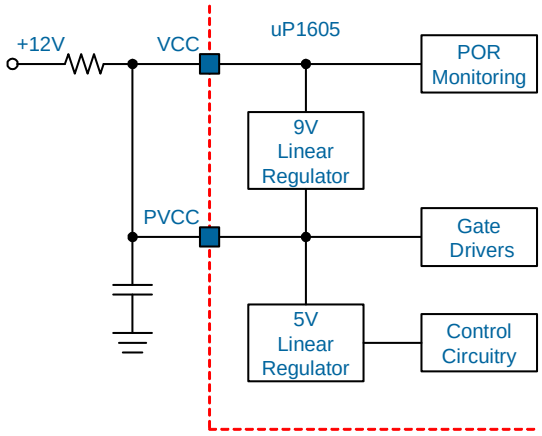


Figure 2. Supply Voltage Configuration for 9V Driving.

The 5V linear regulator works with PVCC input and generates 5VCC for internal control circuitry. No external bypass capacitor is required for filtering the 5VCC voltage.

Bootstrap diodes are embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required.

Chip Enable Oscillation Frequency Programming

A resistor R_{RT} connected to RT/EN pin programs the oscillation frequency as:

$$f_{OSC} = \frac{10000}{R_{RT}(k\Omega)} \quad (kHz)$$

Figure 3 shows the relationship between oscillation frequency and R_{RT}.

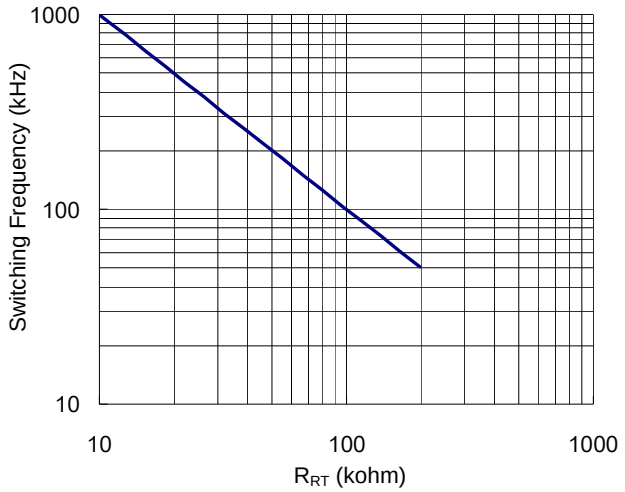


Figure 3. Switching Frequency vs. R_{RT}.

When released, the RT/EN pin voltage is regulated at 1V. Pulling the RT/EN pin to ground shuts down the uP1605.

Voltage Control Loop

Figure 4 shows the simplified voltage control loop of uP1605. VREF is a reference voltage output with 1% accuracy and up to 1mA sourcing capability. RSET is an open drain output that is controlled by VID pin. RSET is pulled to FBRTN when VID = 1 and is set high impedance when VID = 0. Therefore, the reference input voltage at REFIN pin is calculated as:

$$V_{REFIN} = V_{REF} \times \frac{R2}{R1+R2} \quad \text{for VID = 0}$$

$$V_{REFIN} = V_{REF} \times \frac{R2 // R3}{R1+(R2 // R3)} \quad \text{for VID = 1}$$

Users can control VID pin to get two reference voltage levels.

The current-limited buffer receives input at the VREFIN pin and output a voltage source at SS pin. The output capability of the buffer is limited to 20uA during soft start and 210uA after soft start end. A capacitor C_{SS} connected from SS to FBRTN sets the voltage slew rate.

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}} = \frac{20uA}{C_{SS}} \quad \text{during soft start.}$$

$$\frac{dV_{SS}}{dt} = \frac{I_{SS}}{C_{SS}} = \frac{210uA}{C_{SS}} \quad \text{after soft start end.}$$

These slew rates are used to control the output voltage slew at soft start and V_{REFIN} jumping respectively.

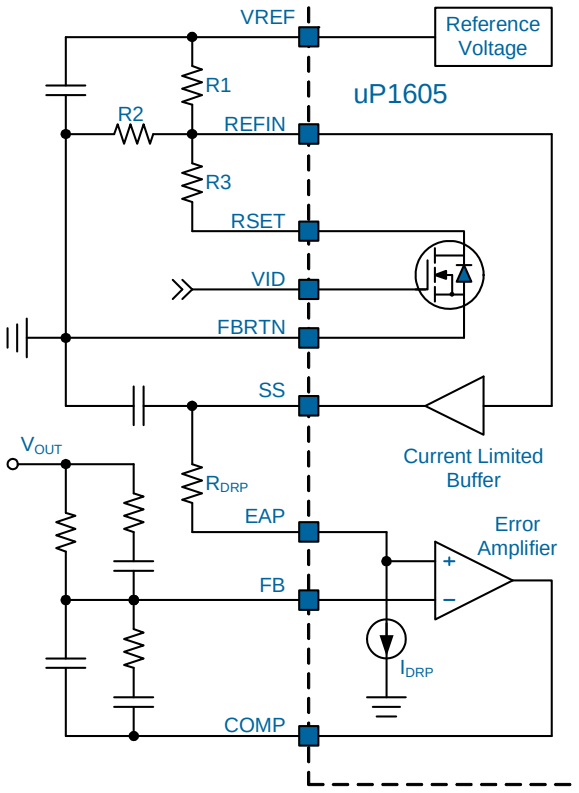


Figure 4. Voltage Control Loop

The FB voltage is tightly regulated to the positive input of the error amplifier, EAP. The output current is sensed and mirrored to the EAP pin, resulting in a voltage droop between SS and EAP.

$$V_{EAP} = V_{SS} - R_{DRP} \times I_{DRP}$$

where I_{DRP} is a current signal proportional to output current. Consequently, at steady state, the output voltage can be expressed as:

$$V_{OUT} = V_{REF} \times \frac{R2}{R1+R2} - R_{DRP} \times I_{DRP} \quad \text{for VID = 0}$$

$$V_{OUT} = V_{REF} \times \frac{R2 // R3}{R1+(R2 // R3)} - R_{DRP} \times I_{DRP} \quad \text{for VID = 1}$$

Soft Start

The uP1605 initiates its soft start cycle when the RT/EN pin released from ground once the POR is granted as shown in Figure 5. As mentioned in the above section, slew rate of voltage transition at SS and output voltage during soft start and V_{REFIN} jumping is controlled by the capacitor connected from SS to FBRTN. This reduces inrush current to charge/discharge the large output capacitors during soft start and VID changing and prevents

OCP, OVP/UVP false trigger.

The SS buffer sinking/sourcing capability is limited to 20uA during soft start and 210uA after soft start end. Therefore, the slew rate of voltage ramping up/down at SS, EAP and FB pin during soft start or VID changing is calculated as:

$$\frac{dV_{SS}}{dt} = \frac{dV_{EAP}}{dt} = \frac{dV_{FB}}{dt} = \frac{20uA}{C_{SS}}$$ during soft start.

$$\frac{dV_{SS}}{dt} = \frac{dV_{EAP}}{dt} = \frac{dV_{FB}}{dt} = \frac{210uA}{C_{SS}}$$ after soft start end.

A limited current source I_{SS} is used to charge/discharge C_{SS} when VID changes.

The RT/EN pin is released and enables the uP1605 at T0. There is a 200us time delay (T0 ~ T1) before the current source I_{SS} begins charging the C_{SS}. The SS, EAP, and output voltage V_{OUT} are kept zero during (T0 ~ T1). The V_{SS}, V_{EAP}, and V_{OUT} ramp up to boot up voltage V_{BOOT} = 1.2V(0.9V) during time (T1 ~ T2). The uP1605 inserts a time delay (T2 ~ T3) for the VID to get valid. The V_{SS}, V_{EAP}, and V_{OUT} ramp to its target value according to VID status during (T3 ~ T4). At T5, the VID changes and V_{SS}, V_{EAP} and V_{OUT} ramp to its new taget.

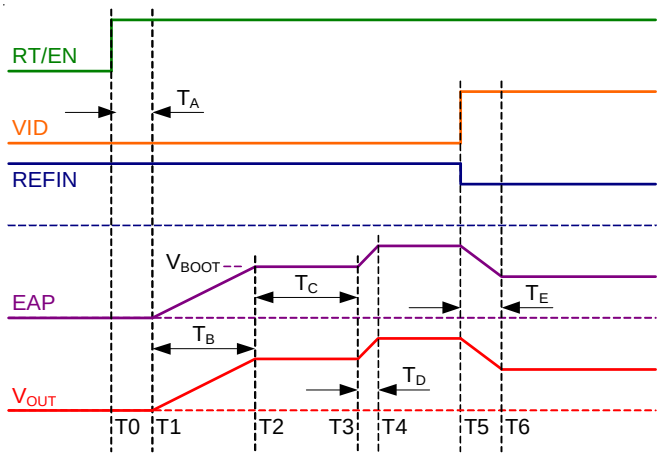


Figure 5. Typical Soft Start Cycle, R_{DRP} = 0Ω

Before time delay T3, the I_{SS} is limited to 20uA. After that, the I_{SS} is limited to 210uA. Consequently, critical time periods are calculated as:

T_B = (T2 - T1) = 1.2V(0.9V) x C_{SS} / 20uA

T_D = (T4 - T3) = |V_{REFIN} - 1.2V(0.9V)| x C_{SS} / 210uA

T_E = (T6 - T5) = |ΔV_{REFIN}| / 210uA

T_A = (T1 - T0) = 200us and T_C = (T3 - T2) = 1.2ms are fixed delay and can not be adjusted externally.

The uP1605 features pre-bias start-up capability. If the output voltage is pre-biased with a voltage, say V_{BIAS}, that accordingly makes V_{FB} higher than reference voltage ramping V_{EAP}. The error amplifier keeps V_{COMP} lower than the valley of the sawtooth waveform and makes PWM comparators output low until the ramping V_{EAP} catches up the feedback voltage. The uP1605 keeps both upper and lower MOSFETs off until the first pulse takes place.

Output Current Sensing

Figure 6 illustrates the output current sensing block of the uP1605. The voltage V_{CS} across the current sensing capacitor C_{CS} can be expressed as:

$V_{CS} = I_{OUT} \times R_{DC} / 2$

if the following condition is true.

$2 \times L / R_{DC} = R_{CSP} \times C_{CS}$

where L is the output inductor of the buck converter, R_{DC} is the parasitic resistance of the inductor, R_{CSP} and C_{CS} are the external RC network for current sensing.

The GM amplifier will source a current I_{CSN} to the CSN pin to let its inputs virtually short circuit.

$I_{CSN} \times R_{CSN} = V_{CS}$

Therefore the output current signal I_{CSN} can be expressed as:

$$I_{CSN} = \frac{I_{OUT} \times R_{DC}}{2 \times R_{CSN}}$$

The output current signal I_{CSN} is used as droop tuning, automatic phase reduction, and output over current protection. Please see the related section for details.

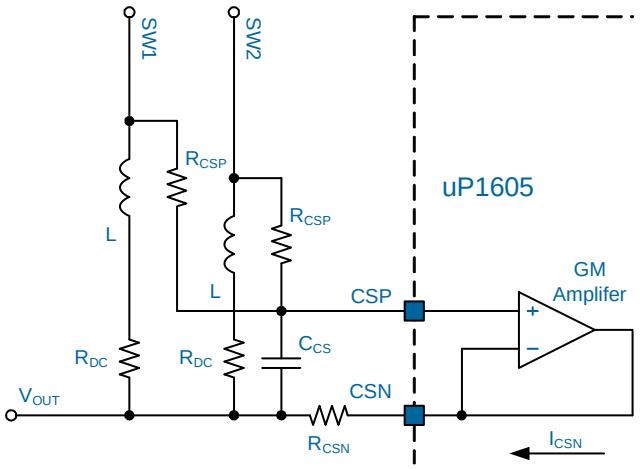


Figure 6. Output Current Sensing of uP1605.

The sourcing capability of the GM amplifier is 100uA. It is recommended to scale ***I_{CSN} = 30uA*** at rated output current and set the OCP current as twice the rated output current. Take a 60A converter for example. Assume R_{DC} = 2mΩ,

select the sense resistor according to

$$R_{CSN} = \frac{60A \times 2m\Omega}{2 \times 30uA} = 2k\Omega$$

Over Current Protection

The sensed current signals are monitored for over current protection. If I_{CSN} is higher than 60uA, the over current protection OCP is activated. Take the above case for example, the OCP level is calculated as:

$$I_{OCP} = \frac{2 \times 60uA \times 2k\Omega}{2m\Omega} = 120A$$

The OCP is of latch-off type and can be reset by toggling RT/EN or VCC POR.

Current Balance

The uP1605 extracts phase currents for current balance by parasitic on-resistance of the lower switches when turned on as shown in Figure 7.

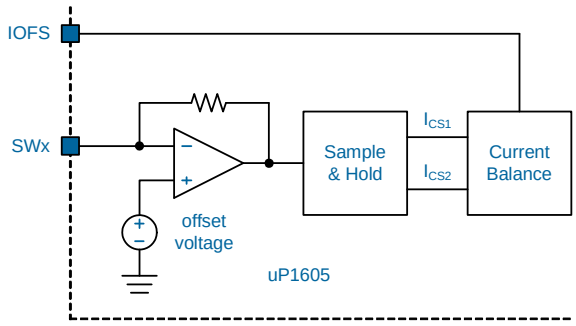


Figure 7. $R_{DS(ON)}$ Current Sensing Scheme

The GM amplifier senses the voltage drop across the lower switch and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = I_{LX} \times R_{DS(ON)} \times 10^{-3} + 6.6uA$$

where I_{LX} is the phase X current in Ampere, $R_{DS(ON)}$ is the on-resistance of low side MOSFET in Ω, 6.6uA is a constant to compensate the offset voltage of the current sensing circuit.

The uP1605 fine tunes the duty cycle of each channel for current balance according to the sensed inductor current signals as shown in Figure 8. If the current of channel 1 is smaller than the current of channel 2, the uP1605 increases the duty cycle of the corresponding phase to increase its phase current accordingly, vice verse.

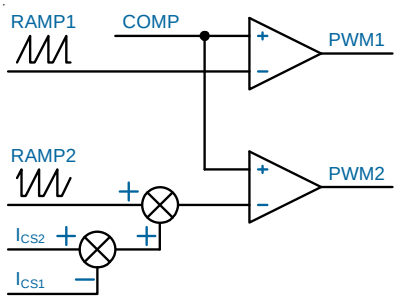


Figure 8. Current Balance Scheme of uP1605.

Automatic Phase Reduction

The uP1605 features automatic phase reduction that turns off phase 2 at light load condtion and reduces both switching and conduction losses. The automatic phase reduction maintains high power conversion efficiency over the output current range.

The output current is sensed and mirrored to PSI pin as:

$$I_{PSI} = I_{CSN} = \frac{I_{OUT} \times R_{DC}}{2 \times R_{CSN}}$$

The I_{PSI} creates a voltage V_{PSI} as:

$$V_{PSI} = R_{PSI} \times I_{PSI} = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

The uP1605 operates in dual phase if V_{PSI} is higher than 0.6V and in single phase if V_{PSI} is lower than 0.4V. There is a 200mV hystersis at the phase change threshold. There is a 1ms delay when entering single phase operation and no time delay when entering dual phase operation. When operating single phase, both HG2 and LG2 are turned off.

Take the above case for example, with R_{PSI} = 80kΩ, the threshold level of output current for entering single phase operation is calculated as:

$$0.4V = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

$$I_{OUT} = \frac{0.4V \times 2 \times 2k\Omega}{2m\Omega \times 80k\Omega}$$

$$I_{OUT} = 10A$$

The threshold level of output current for entering dual phase operation is calculated as:

$$0.6V = \frac{I_{OUT} \times DCR \times R_{PSI}}{2 \times R_{CSN}}$$

$$I_{OUT} = \frac{0.6V \times 2 \times 2k\Omega}{2m\Omega \times 80k\Omega}$$

$$I_{OUT} = 15A$$

Note that when operated in single phase, the rated current is reduced to ***80 percents*** of normal level. Continuous demanding high current may damage the converter.

Connect PSI pin to VREF to disable the automatic phase reduction function. Since the VREF has no sinking capability, make sure the external loading is higher than 100uA when connecting PSI pin to VREF. Otherwise, VREF may loss its regulation.

Over Voltage and Under Voltage Protection

The FB voltage is continuously monitored for over voltage and under voltage protection. The uP1605 asserts over voltage protection if $V_{FB} > V_{SS}$ + 300mV and turns on the lower MOSFETs and shuts down the converter. The uP1605 asserts under voltage protection if $V_{FB} < V_{SS}$ - 300mV and shuts down the converter. The UVP function is disabled during soft start.

Both UVP and OVP are latch-off type and can be reset only by toggling the RT/EN pin ro by VCC power on reset.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC/PVCC ---------- -0.3V to +15V
BOOTx to SWx ---------- -0.3V to +15V
SWx to GND
DC ---------- -0.7V to 15V
< 200ns ---------- -8V to 30V
BOOTx to GND
DC ---------- -0.3V to VCC + 15V
< 200ns ---------- -0.3V to 42V
UGx to SWx
DC---------- -0.3V to (BOOTx - SWx +0.3V)
<200ns ---------- -5V to (BOOTx - SWx + 0.3V)
LGx to GND
DC ---------- -0.3V to + (VCC + 0.3V)
<200ns ---------- -5V to (VCC + 0.3V
Input, Output or I/O Voltage ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN4x4 - 24L θ_{JA} ---------- 40°C/W
VQFN4x4 - 24L θ_{JC} ---------- 6°C/W
Power Dissipation, P_D @ TA = 25°C
VQFN4x4 - 24L ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{CC} ---------- 10.8V to 13.2V

Electrical Characteristics

(V_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		10.8	--	13.2	V
Supply Current	I_{CC}	HG and LG Open; V_{CC} = 12V, Switching	3	5	7	mA
Quiescent Supply Current	I_{CC_Q}	No Switching, I_{PCC} = 0mA	2	4	6	mA
Regulated Supply Voltage	V_{PCC}	RT/EN = 0V, I_{PCC} = 0mA	8	9	10	V
POR Threshold	V_{CCRTH}		8	9	10	V
POR Hysteresis	V_{CCHYS}		--	0.8	--	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Chip Enable/Frequency Setting						
RT/EN Sourcing Current	$I_{RT/EN}$	RT/EN = GND.	--	210	--	uA
RT/EN Voltage	$V_{RT/EN}$	$R_{RT/EN}$ = 33kΩ	0.94	1	1.06	V
Switching Frequency Setting Range			50	--	1000	kHz
Free Run Switching Frequency	f_{OSC}	$R_{RT/EN}$ = 33kΩ	270	300	330	kHz
Switching Frequency Accuracy	Δf_{OSC}	f_{OSC} = 200kHz ~ 500kHz	-15	--	15	%
Soft Start						
Soft Start Current	I_{SS}	During soft start.	16	20	24	uA
	I_{SS}	After soft start end.	160	210	270	
Boot Up Voltage	V_{BOOT}	for uP1605P, Guaranteed by design.	1.188	1.2	1.212	V
		for uP1605Q, Guaranteed by design.	0.891	0.9	0.909	
Boot Up Hold Up Time	T_C	Guaranteed by design.	0.6	1.2	1.8	ms
Oscillator						
Maximum Duty Cycle			80	85	90	%
Minimum Duty Cycle			--	0	--	%
Ramp Amplitude	ΔV_{OSC}	V_{CC} = 12V.	3	3.5	4	V
Power Saving Mode						
Threshold Voltage for Entering Dual Phase	V_{PSI}	V_{PSI} rising.	0.55	0.6	0.65	V
Hysteresis Voltage for Entering Single Phase	ΔV_{PSI}	V_{PSI} falling.	--	200	--	mV
Reference Voltage						
Reference Voltage Accuracy	V_{REF}	I_{REF} = 100uA	1.98	2.00	2.02	V
Reference Voltage Load Regulation	ΔV_{REF}	I_{REF} = 0 ~ 2mA	-5	--	5	mV
Output Voltage Accuracy	V_{FB}	V_{REFIN} - V_{FB}, V_{CC} = 12V, No Load, R_{DRP} = 0Ω, V_{REFIN} = 0.8V ~ 1.6V.	-2	0	2	mV
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by design.	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF, Guaranteed by design.	20	--	--	MHz
Slew Rate	SR	Guaranteed by design.	15	20	--	V/us
Maximum Current (Sink & Source)	I_{COMP}	V_{COMP} = 1.6V	1.5	2.0	--	mA
Total Current Sense						
Maximum Sourcing Current	I_{CSN_MAX}		100	--	--	uA
GM Amplifier Offset			-1	0	1	mV
Over Current Protection Threshold Level	I_{CSN_OCP}		55	60	65	uA
Droop Accuracy		I_{DRP}/I_{CSN}	90	100	110	%
PSI Accuracy		I_{PSI}/I_{CSN}	90	100	110	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Phase Current Sense						
Trans-conductance			--	1.0	--	mS
IOFS Voltage	V_{OFS}	100kΩ from IOFS to VREF	1.45	1.5	1.55	V
		100kΩ from IOFS to GND	0.45	0.5	0.55	
VID Control Input						
Logic High Threshold Level	V_{IL}		2	--	--	V
Logic Low Threshold Level	V_{IL}		--	--	0.4	V
On Resistance of RSET MOSFET	R_{RSET}	VID = High	10	20	40	Ω
Leakage of RSET Pin	I_{RSET}	V_{RESET} = 2V, VID = 0V	--	--	0.1	uA
Gate Driver						
Upper Gate Sourcing	R_{HG_SRC}	I_{HG} = 100mA sourcing	--	3	6	Ω
Upper Gate Sinking	R_{HG_SNK}	I_{HG} = 100mA sinking	--	2	4	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = 100mA sourcing	--	2.5	5	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 100mA singking	--	1.3	2.6	Ω
Dead Time	T_{DT}		--	30	--	ns
Protection						
Over Voltage Protection		V_{FB} - V_{SS}	250	300	350	mV
Under Voltage Protection		V_{FB} - V_{SS}	-350	-300	-250	mV
Over Temperature Protection			--	150	--	°C
Over Temperature Hysteresis			--	20	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

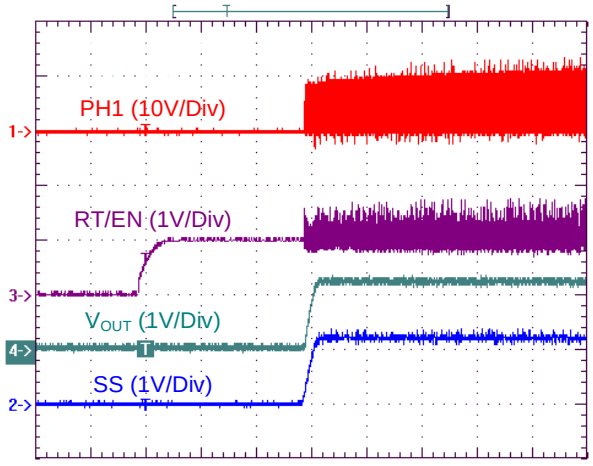
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

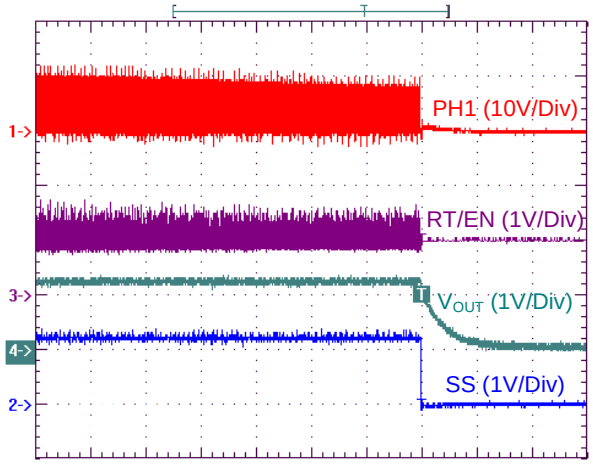
Typical Operation Characteristics

Power On Waveforms



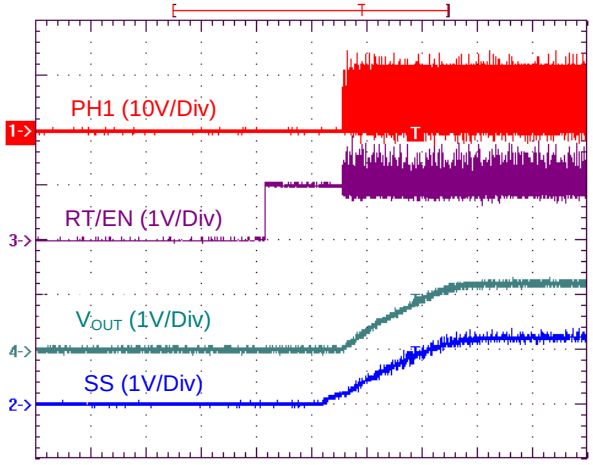
Time (2ms/Div)
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 40A

Power Off Waveforms



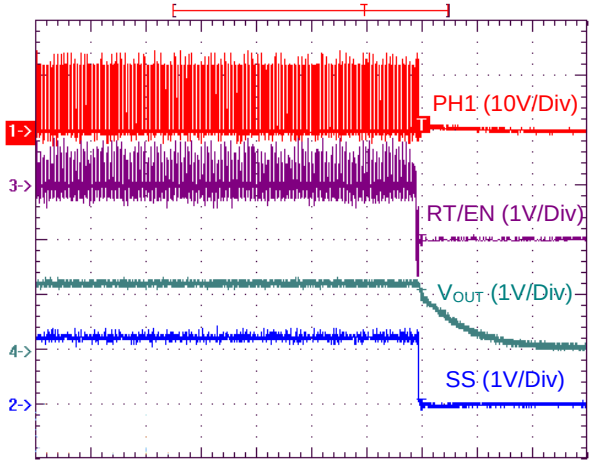
Time (200us/Div)
V_{IN} = 12V, I_{OUT} = 40A

Turn On Waveforms



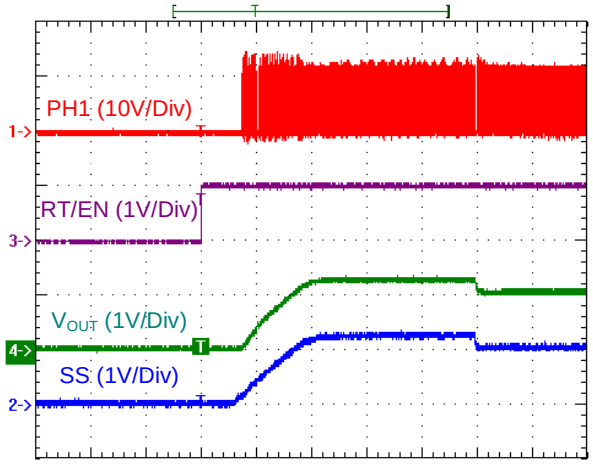
Time (200us/Div)
V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 40A

Turn Off Waveforms



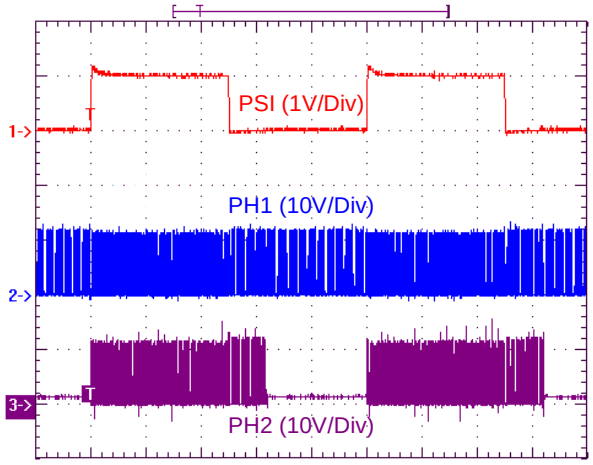
Time (100us/Div)
V_{IN} = 12V, I_{OUT} = 40A

Turn On Waveforms



Time (400us/Div)
V_{IN} = 12V, V_{OUT} = 1.0V, I_{OUT} = 40A

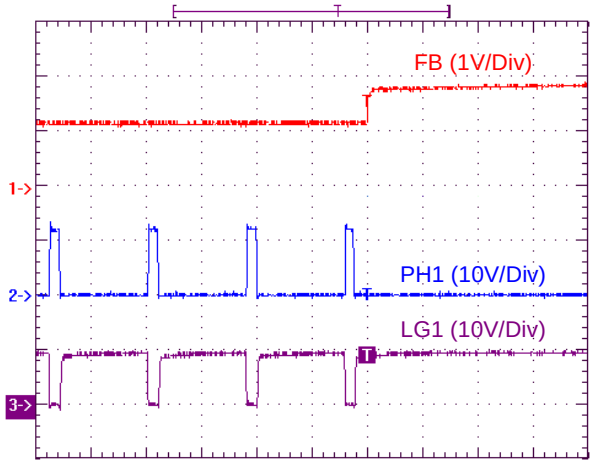
PSI Function



Time (2ms/Div)
V_{IN} = 12V, I_{OUT} = 0A to 40A

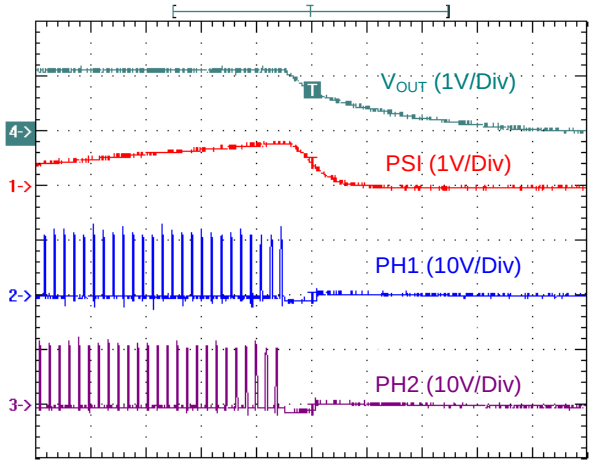
Typical Operation Characteristics

Over Voltage Protection



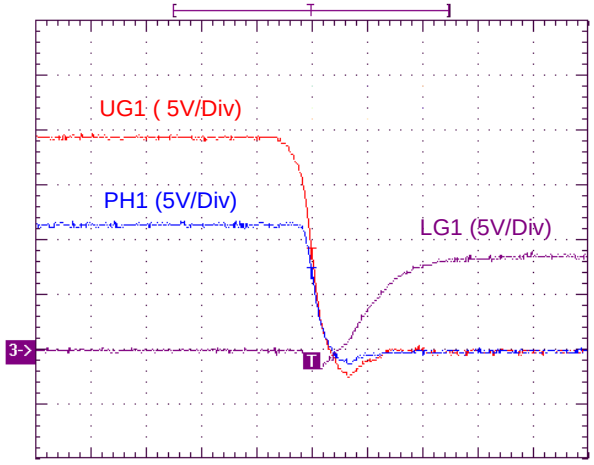
Time (2us/Div)

Over Current Protection



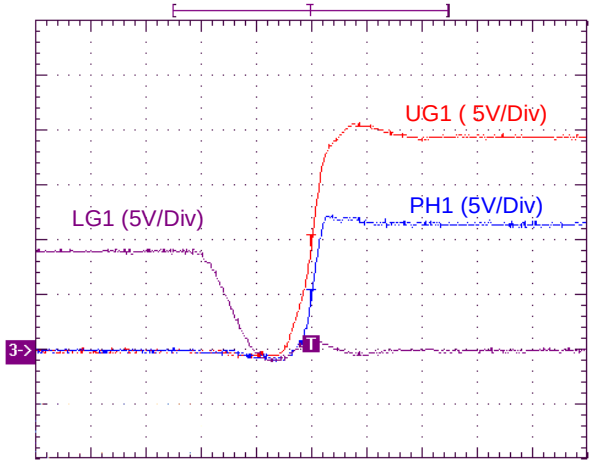
Time (20us/Div)

UG1 Falling Waveforms



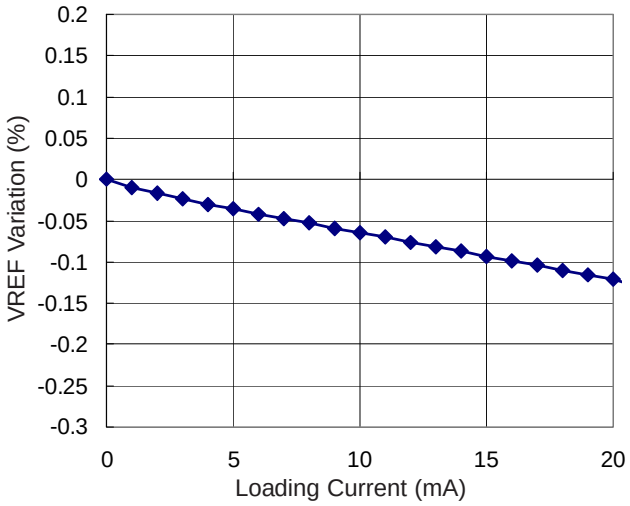
Time (40ns/Div)
V_{IN} = 12V, I_{OUT} = 40A, 20MHz Bandwidth Limited

UG1 Rising Waveforms

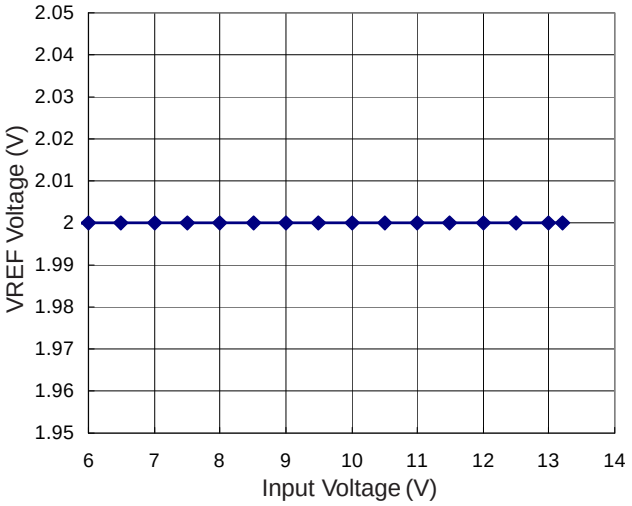


Time (40ns/Div)
V_{IN} = 12V, I_{OUT} = 40A, 20MHz Bandwidth Limited

VREF Load Regulation

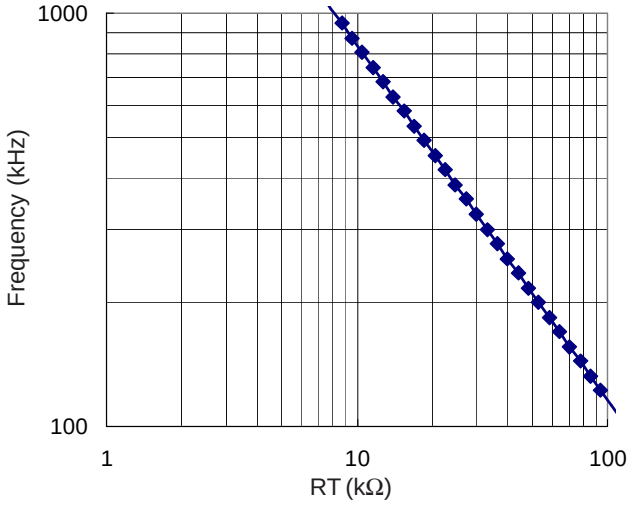


VREF Line Regulation

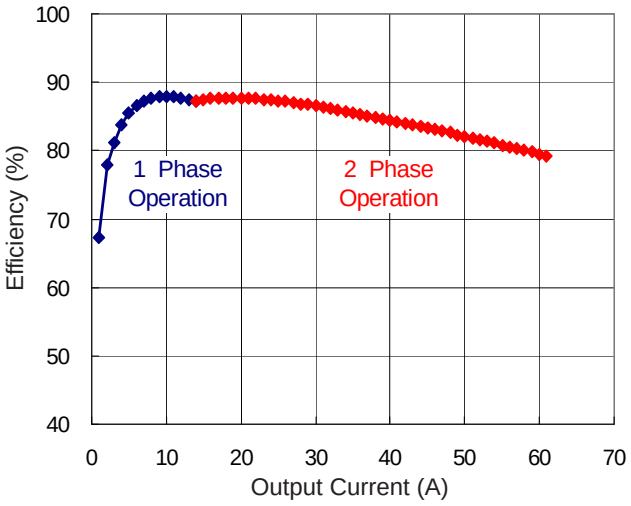


Typical Operation Characteristics

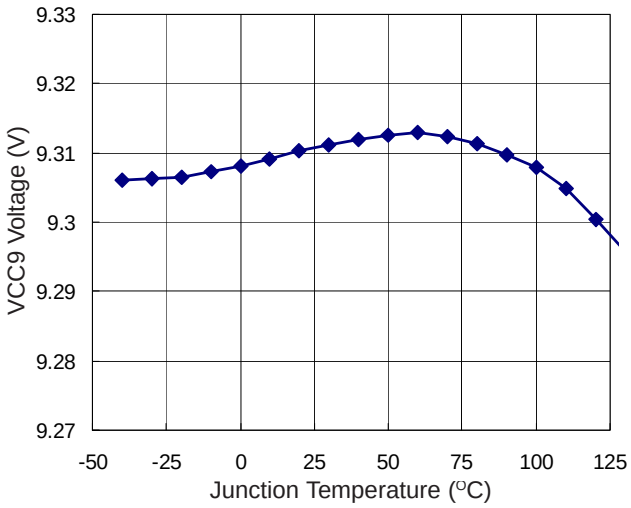
Frequency vs. RT



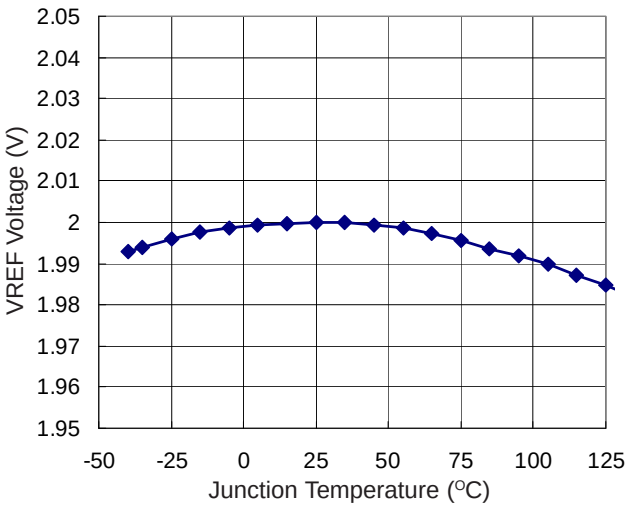
Efficiency vs. Output Current with Auto PSI



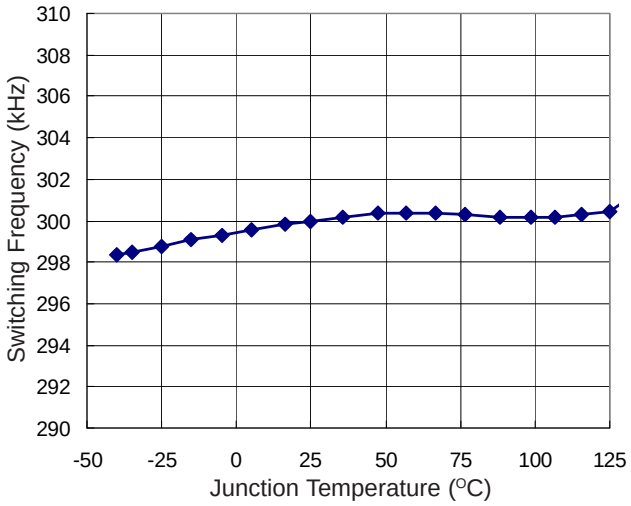
VCC9 Voltage vs. Tempereture



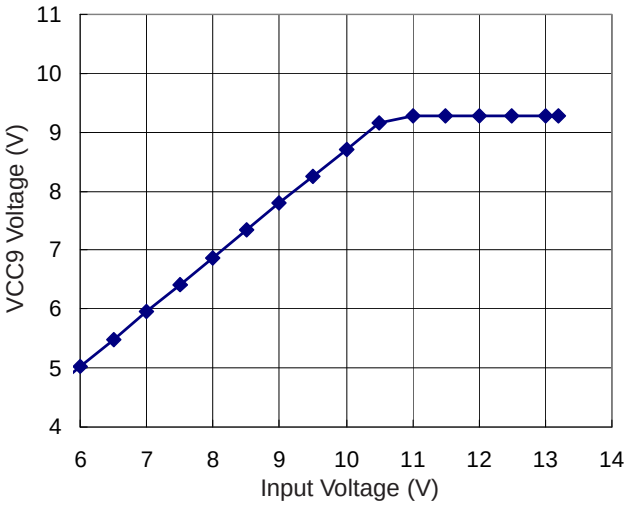
VREF Voltage vs. Temperature



Switching Frequency vs. Tempereture



VCC9 Line Regulation



FBRTN Configuration

Since the reference voltage V_{REF} is measured with respective to FBRTN, connect circuits related to VREF, REFIN, and SS pin to FBRTN locally with short traces as shown in the *Typical Application Circuit*.

Total Current Sensing

In the real application, PCB trances are not ideal and have certain parasitic resistances R_{PCB1} and R_{PCB2} as shown in Figure 1. When these parasistic resistances are not identical, the voltages at inductor terminals are not the same, contributing meausrement error on total current sensing. Two 1Ω resistors, connecting directly to inductor terminals are recommended to elimiate the effects of parasitic resistance.

A 0.1uF capacitor C_{BYP} is also recommended to bypassing noise when the uP1605 is far away from the output inductors. Place the C_{BYP} physically near the IC.

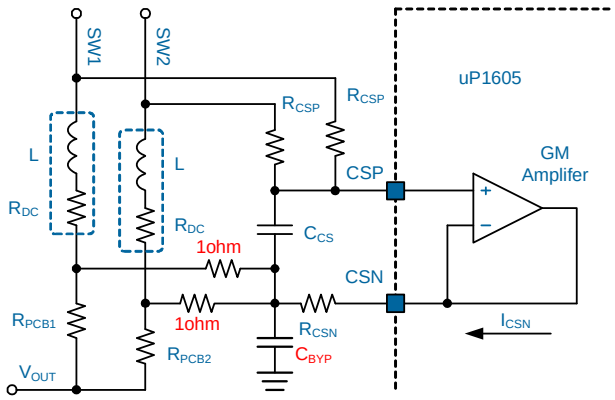


Figure 1. Parasitic Resistance of PCB

Component Selection Guidelines

The selection of external component is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The desired amount of ripple current and operating frequency largely determines the inductor value. Finally, C_{IN} is selected for its capability to handle the large RMS current into the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specification.

Power MOSFET Selection

The uP1605 requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is supplied by PVCC pin that is the output of internal 9.0V LDO regulator.

Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the uP1605 may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 40ns or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP1605 is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}};\ D_{LOW} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LOW} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LOW}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the upper MOSFET includes an additional term for switching losses, which are largest at high input voltages. The lower MOSFET losses are greatest when the bottom duty cycle is near 100%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are mainly dissipated by the uP1605 and don't heat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_{G\_C} = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS\_UP}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LOW} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP1605, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based on the considerations of inductance, rated current, size requirements and DC resistance (DCR).

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 20% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40°C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Input Capacitor Selection

The synchronous-rectified Buck converter draws pulsed current with sharp edges from the input capacitor, resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(REMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The equivalent ripple current into the output capacitor is half of the inductor ripple current while the equivalent frequency is double of phase operation frequency due to two phase operation The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} = \frac{\Delta I_L}{2} \left(ESR + \frac{1}{16 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for

filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper MOSFET turns on, the PHASE node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + V_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.47µF to 1uF, X5R or X7R dielectric capacitor is adequate.

Feedback Loop Compensation

Figure 2 highlights the voltage-mode control loop for a synchronous-rectified buck converter consisting of uP1605. The control loop includes a compensator and a modulator, where the modulator consists of the PWM comparator, the power stage amplifier and the output filter; the compensator consists of the feedback network, the error amplifier and compensating network. A well-designed feedback loop tightly regulates the feedback voltage (V_{FB}) to the reference voltage V_{REF} with fast response to load/line transient and good stability. The goal of the compensation network is to provide the highest 0dB crossing frequency and adequate phase margin (greater than 45 degrees). It is also recommended to manipulate loop frequency response that its gain crosses over 0dB at a slope of -20dB/dec.

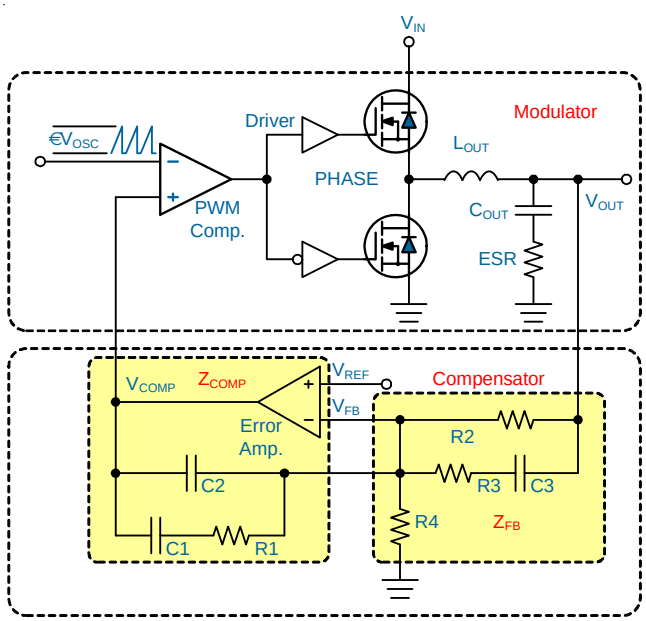


Figure 2. Voltage-Mode Control Loop of uP1605.

Modulator Break Frequency Equations

The error amplifier output (V_{COMP}) is compared with the oscillator (OSC) sawtooth waveform to provide a pulse-width modulated (PWM) waveform with an amplitude of V_{IN} at the PHASE node. The PWM waveform is smoothed by the output filter (L_{OUT} and C_{OUT}). The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC Gain and the output filter (L_{OUT} and C_{OUT}), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as:

$$F_{LC} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The ESR zero is contributed by the ESR associated with the output capacitor. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements as described in the later sections. The ESR zero of the output capacitor expressed as:

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

Figure 3 illustrates frequency response of a typical modulator using uP1605.

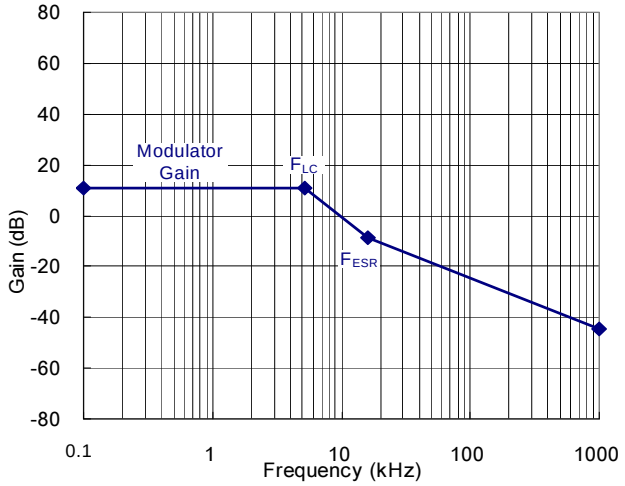


Figure 3. Frequency Response of Modulator.

2) Compensator Frequency Equations

Figure 4 illustrates a type II compensation network using uP1605. The compensation network consists of the error amplifier and the impedance networks Z_{FB} and Z_{COMP}.

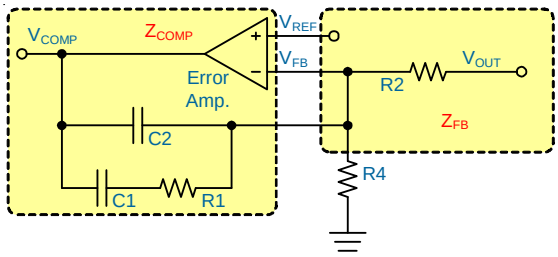


Figure 4. Type II Compensation Network Using uP1605.

The compensator transfer function is the small-signal transfer function of V_{COMP}/V_{OUT}. To get the transifer function, we assume the error amplifier has infinite DC gain and bandwidth. The assumption brings $V_{FB} = V_{REF}$ at any conditions. Consequently, the transfer function can be written as:

$$\frac{V_{COMP}}{V_{OUT}} = \frac{Z_{COMP}}{Z_{FB}} = \frac{s \times R1 \times C1 + 1}{s \times R2(C1 + C2)(sR1 \times \frac{C1 \times C2}{C1 + C2} + 1)}$$

This function is dominated by a Mid-Band Gain and compensation network Z_{COMP}, with a pole at F_{P1} and a zero at F_{Z1}. The Mid-Band Gain of the compensation is expressed as:

$$Mid\_Band\_Gain = \frac{R1}{R2}$$

The equations below relate the compensation network's pole and zero to the components (R1, C1, and C2) in Figure 5.

$$F_{P1} = \frac{1}{2\pi \times R1 \times (\frac{C1 \times C2}{C1 + C2})} ; \quad F_{Z1} = \frac{1}{2\pi \times R1 \times C1}$$

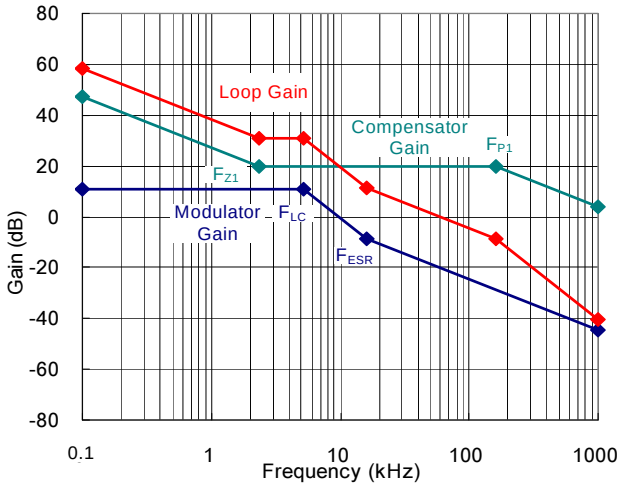


Figure 5. Frequency Response of Type II Compensation.

Figure 6 shows the DC-DC converter's gain vs. frequency. Careful design of Z_{COMP} and Z_{FB} provides tight regulation and fast response to load/line transient with good stability. Follow the guidelines for locating the poles and zeros of the compensation network.

1. Pick Mid-Band Gain (R1/R2) for desired converter bandwidth.
2. Place Zero (C1) below LC double pole (~20% P_{LC}).
3. Place Pole (C2) at half the switching frequency.
4. Check gain against error amplifier open loop gain.
5. Estimate phase margin - repeat if necessary.

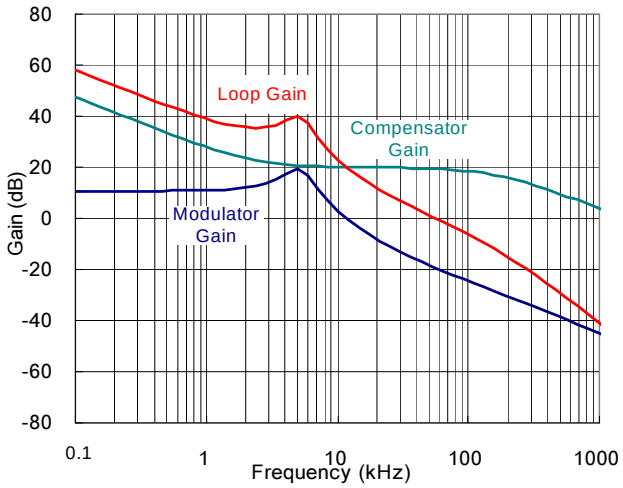


Figure 6. Frequency Response of Type II Compensation.

Design Example

As a design example, take a power supply with the following specifications:

V_{IN} = 10.8V to 13.2V (12V nominal), V_{OUT} = 1.2V ±5%, $I_{OUT(MAX)}$ = 40A, f_{OSC} = 300kHz, ΔV_{OUT} = 20mV, bandwidth = 60kHz.

1.) Power Component Selection

First, choose the inductor for about 20% ripple current at the maximum V_{IN}:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

$$\Delta I_L = 40A \times 20\% = \frac{1}{300kHz \times L_{OUT}} \times 1.2V \times (1 - \frac{1.2V}{13.2V})$$

$$L_{OUT} = 0.45\,uH$$

Selecting a standard value of 0.47uH results in a maximum ripple current of 7.7A. The ripple current into output capacitors is 3.9A.

Choose two 1000uF capacitors with 10mΩ ESR in parallel to yield equivalent ESR = 5mΩ. The output ripple voltage is about 20mV accordingly. An optional 22uF ceramic output capacitor is recommended to minimize the effect of ESL in the output ripple.

The modulator DC gain and break frequencies are calculated as:

$$DC\ Gain = 20 \times \log(\frac{V_{IN}}{\Delta V_{OSC}}) = 20 \times \log(\frac{12}{3.5}) = 10.7dB$$

$$F_{LC} = \frac{1}{2\pi\sqrt{0.47 \times 10^{-6} \times 2000 \times 10^{-6}}} = 5.2kHz$$

$$F_{ESR} = \frac{1}{2\pi \times 5 \times 10^{-3} \times 2000 \times 10^{-6}} = 16kHz$$

2.) Compensation

Let V_{REFIN} = 1.2V by selecting adequate voltage divider at REFIN pin. Select R2 = 1Ω and let R4 open.

The modulator gain at zero-crossing frequency (60kHz) is calculated as -20.3dB. This demands a compensator with mid-band gain as 20.3dB. Select R1 as:

$$R1 = 10^{(20.3/20)} \times R2 = 10.35k\Omega$$

Select C1 = 10nF to place F_{Z1} = 1.6kHz, about one fifth of the LC double pole.

Select C2 = 100pF to place F_{P1} = 160kHz, about half of the equivalent switching frequency.The result loop gain vs. frequency relation is shown in Figure 6.

The ESR zero plays an important role in type II compensation. Output capacitors with low ESR and small capacitance push the ESR zero to high frequency band. If the ESR zero is six times higher than the LC double pole, the double pole may cause the loop phase close to 180° and make the control loop unstable. A type II compensation cannot stabilize the loop since it has only one zero.

Type III Compensation

A type III compensation network as shown in Figure 7 that features 2 poles and 2 zeros is necessary for such applications where ESR zero is far away from the LC double pole (F_{LC} > 6x F_{ESR}). Adding a feedforward netwpprl C3 and R3 on original type II compensation network introduces an additional pole-zero pair (Z2 and P2) as illustrated in Figure 19. The new pole-zero pair are expressed as:

$$F_{Z2} = \frac{1}{2\pi \times R3 \times C3};\ F_{P2} = \frac{1}{2\pi \times C3 \times (R2 + R3)}$$

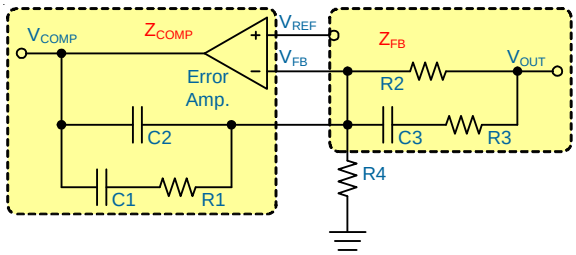


Figure 7. Type III Compensation Network.

While the Mid-Band Gain remains unchanged, the additional pole-zero pair causes a gain boost at the flat gain region. The gain-boost is limited by the ratio (R2 +R3)/ R3. Figures 8 show the DC-DC converter's gain vs. frequency.

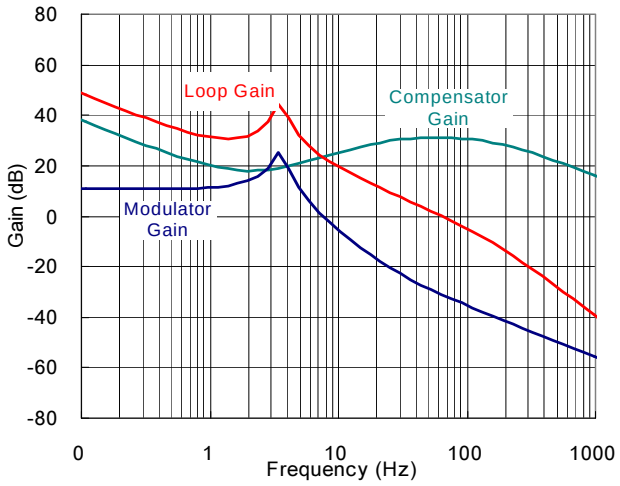


Figure 8. Frequency Response of Type III Compensation.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD}x(ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1605.

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP1605 near the upper and lower MOSFETs with UGATE and LGATE facing the power components. Keep the components connected to noise sensitive pins near the uP1605 and away from the inductor and other noise sources.

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP1605 Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

6 The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

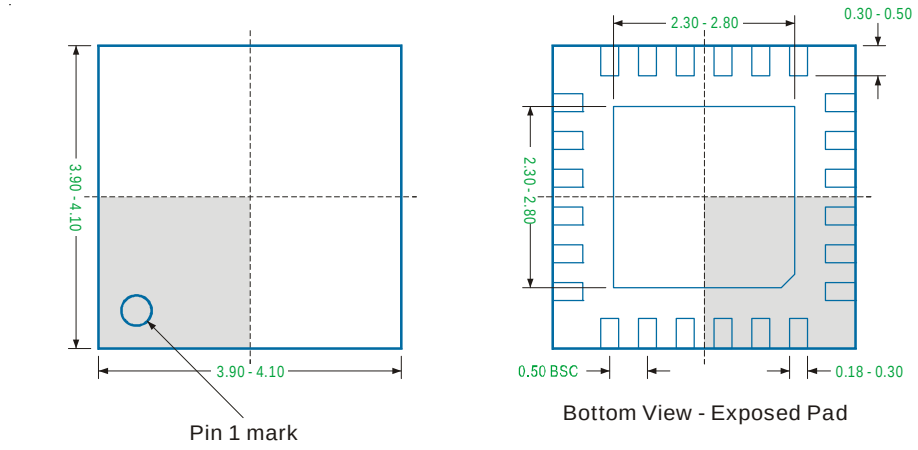
7 The uP1605 sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as possible to the BOOT and PHASE pins.

Package Information

VQFN4x4-24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

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