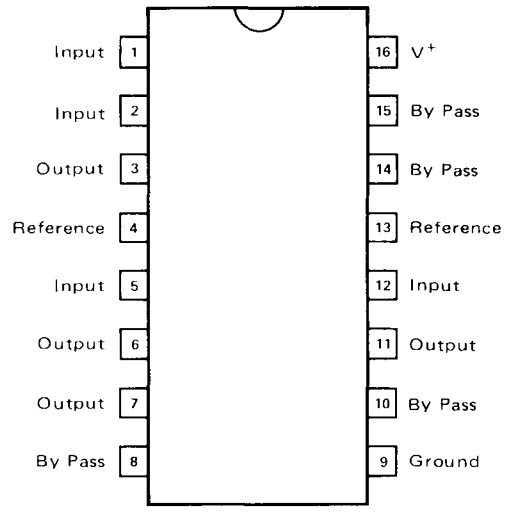
DESCRIPTION

The NE545 is the monolithic implementation of the Dolby-B noise reduction system. This circuit is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licencees of Dolby Labs. Licensing and application information may be obtained from Dolby Labs, London or New York.

PIN CONFIGURATION (Top View)

B PACKAGE

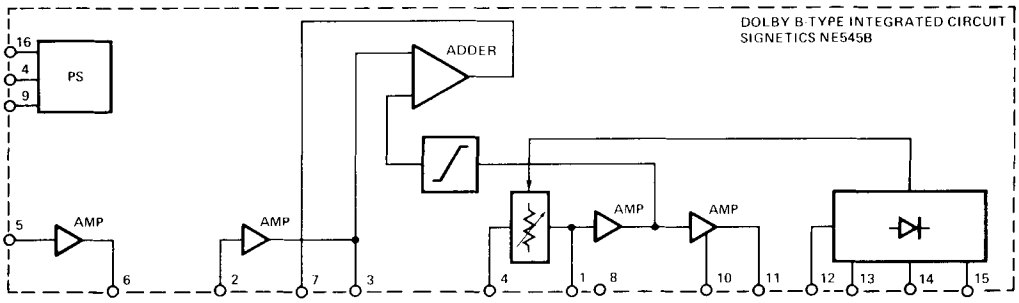


Order Part No. NE545B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	24 Volts
Operation Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	+300°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{CC} = 12 volts, f = 20Hz to 20kHz. All levels referenced to 580mV RMS (0dB) at Pin 3, T_A = +25°C (Unless Otherwise Noted).

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		MIN	TYP	MAX	
Supply Voltage Range		10		20	V
Supply Current			21	30	mA
Voltage Gain (Pins 5—3)	f = 1kHz (Pins 6 & 2 Connected)	23	26	29	dB
Voltage Gain (Pins 3—7)	f = 1kHz, 0dB at Pin 3, Noise Reduction Out	−1	0	+1	dB
Distortion	f = 1kHz, 0dB at Pin 7		0.05	0.1	%
	f = 1kHz, +10dB at Pin 7		0.2	0.5	%
Signal Handling	f = 1kHz Distortion < 0.5%	+10	+12		dB
Signal-To-Noise Ratio	Record (Pins 6 & 2 Connected)	62	65		dB
	Record (Input on Pin 2)	66	70		dB
	Playback (Pins 6 & 2 Connected)	62	70		dB
	Playback (Input on Pin 2)	66	76		dB
Record Mode Frequency Response (at Pin 7)	f = 1.4kHz				
	Input at Pin 5 = 0dB	−2	0	+2	dB
	= −20dB	−17.6	−15.6	−13.6	dB
	= −30dB	−24.5	−22.5	−20.5	dB
	f = 5kHz				
	Input at Pin 5 = 0dB	−2	0	+2	dB
	= −20dB	−18.8	−16.8	−14.8	dB
	= −30dB	−23.8	−21.8	−19.8	dB
	= −40dB	−31.7	−29.7	−27.7	dB
	f = 10kHz				
	Input at Pin 5 = 0dB	−2	0	+2	dB
	= −20dB	−19.4	−17.4	−15.4	dB
	= −30dB	−25.5	−23.5	−21.5	dB
Back-to-Back Frequency Response	Using Typical Record Mode Response	−2	0	+2	dB
Input Resistance	Pin 5	50	100		k ohms
	Pin 2	3.9	5.6	6.7	k ohms
Output Resistance	Pin 6	1.9	2.4	3.1	k ohms
	Pin 3		80	120	ohms
	Pin 7		80	120	ohms

TYPICAL PERFORMANCE CURVES

FIGURE 1
I_{CC} VERSUS V_{CC}

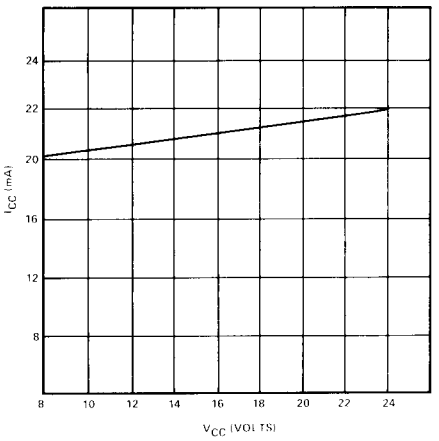


FIGURE 2
VOLTAGE GAIN PIN 1 TO PIN 11

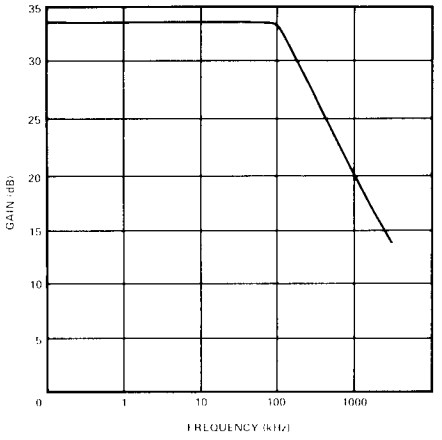


FIGURE 3
VOLTAGE GAIN PIN 1 TO PIN 7

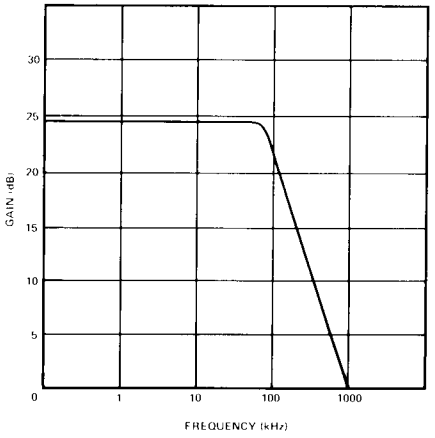


FIGURE 4
VOLTAGE GAIN PIN 5 TO PIN 7

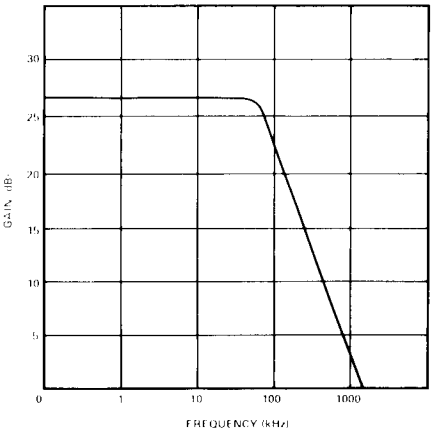


FIGURE 5
VOLTAGE GAIN PIN 5 TO PIN 3

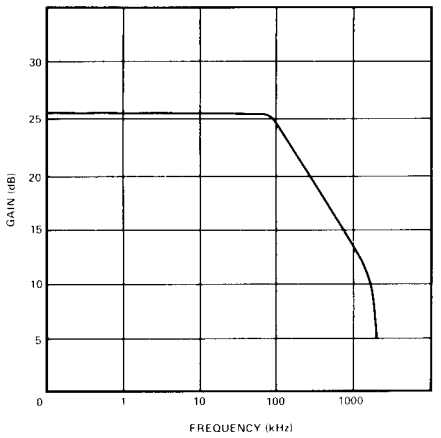
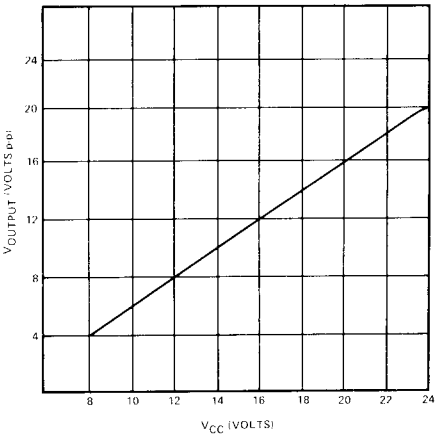


FIGURE 6
PEAK-TO-PEAK OUTPUT SWING
VERSUS V_{CC}



TYPICAL PERFORMANCE CURVES

FIGURE 7
DISTORTION VERSUS FREQUENCY
0dB ENCODE

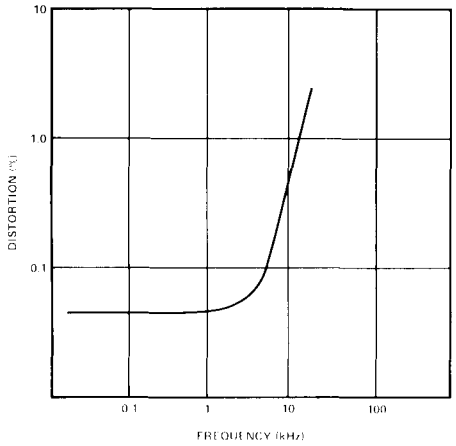


FIGURE 8
DISTORTION VERSUS FREQUENCY
0dB DECODE

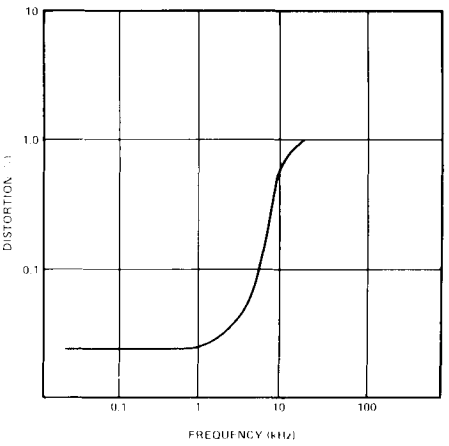


FIGURE 9
DISTORTION VERSUS FREQUENCY
0dB AND +10dB
NOISE REDUCTION OUT

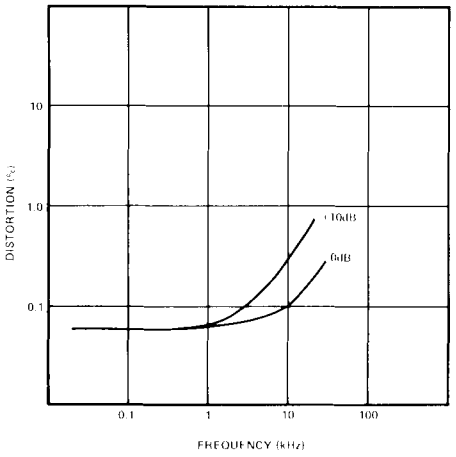


FIGURE 10
DISTORTION VERSUS OUTPUT
1kHz AND 10kHz

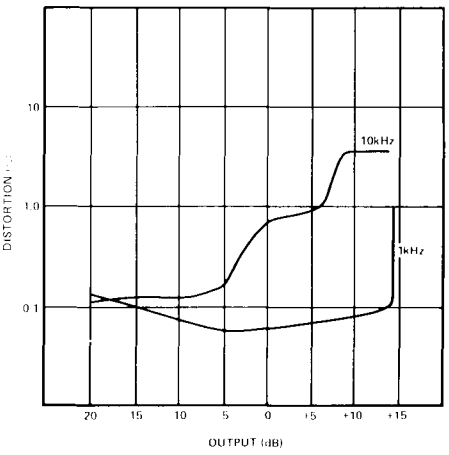


FIGURE 11
BACK-TO-BACK FREQUENCY RESPONSE
VERSUS TEMPERATURE
ENCODE AT –25°C AND –10dB

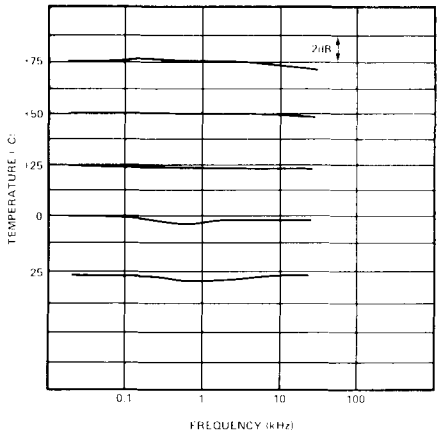
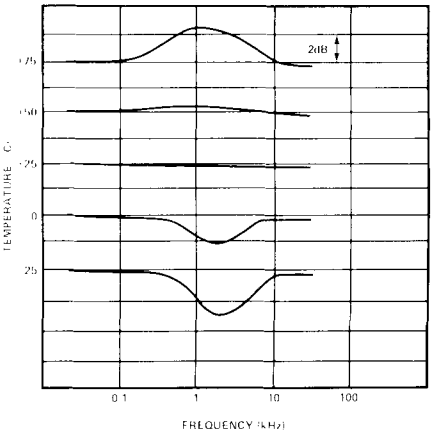


FIGURE 12
BACK-TO-BACK FREQUENCY RESPONSE
VERSUS TEMPERATURE
ENCODE AT +25°C AND –20dB



TYPICAL PERFORMANCE CURVES

FIGURE 13
BACK-TO-BACK FREQUENCY RESPONSE
VERSUS TEMPERATURE
ENCODE AT +25°C AND –30dB

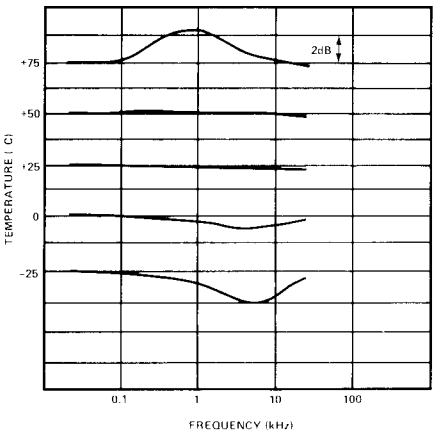


FIGURE 14
BACK-TO-BACK FREQUENCY RESPONSE
VERSUS TEMPERATURE
ENCODE AT +25°C AND –40dB

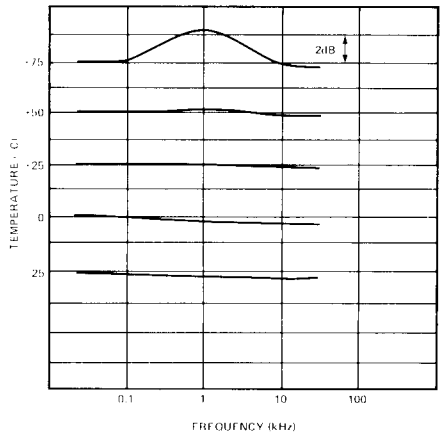


FIGURE 15
LOW LEVEL FREQUENCY RESPONSE

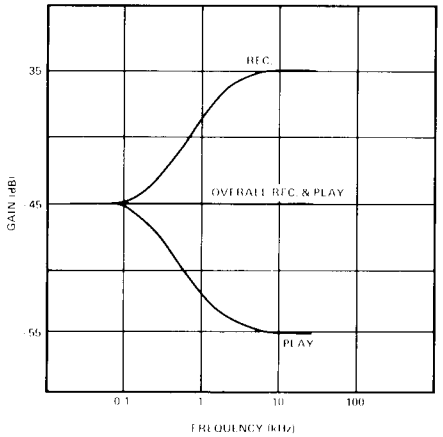


FIGURE 16
MAXIMUM OUTPUT SWING
VERSUS FREQUENCY
REF. = 1% THD

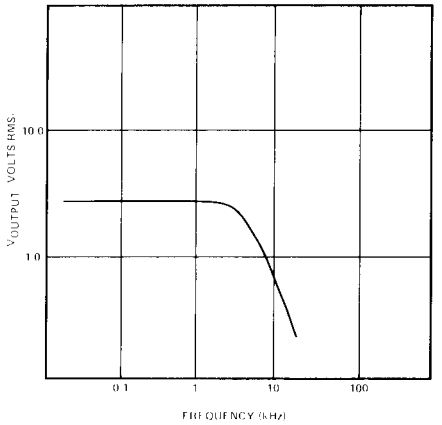


FIGURE 17
ENCODE CHARACTERISTICS

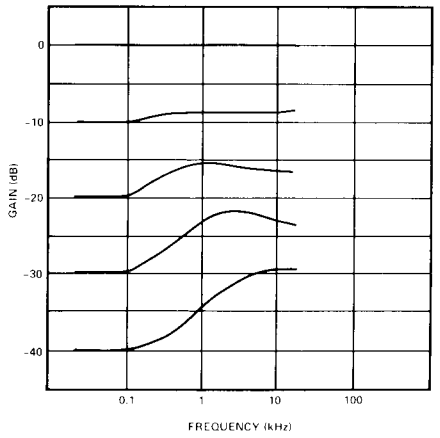
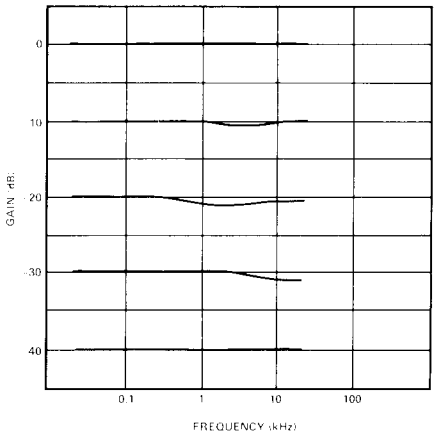


FIGURE 18
LEVEL MISMATCH RESPONSE
2dB LOSS BETWEEN ENCODE AND DECODE



TYPICAL PERFORMANCE CURVES

FIGURE 19
TONE BURST ENCODE
0dB 1kHz

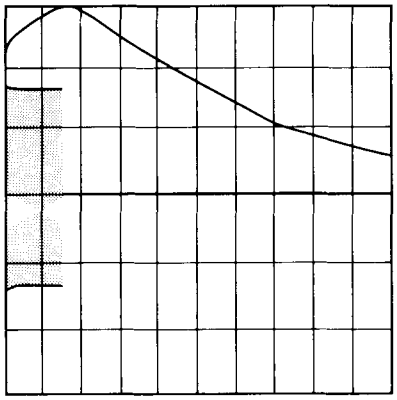


FIGURE 20
TONE BURST ENCODE
−10dB 1kHz

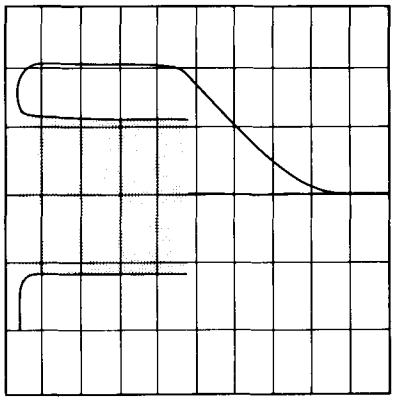


FIGURE 21
TONE BURST ENCODE
−20dB 1kHz

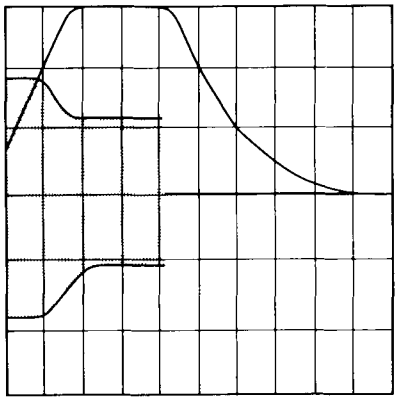
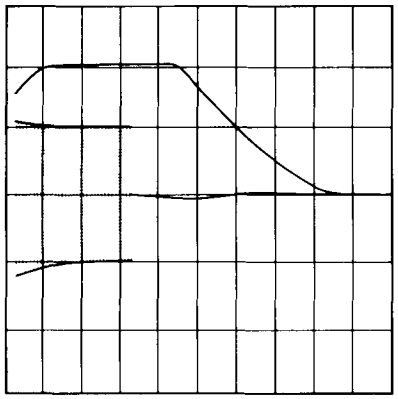


FIGURE 22
TONE BURST ENCODE
−30dB 10kHz



PROCESSOR CHARACTERISTICS ANALYSIS FORM

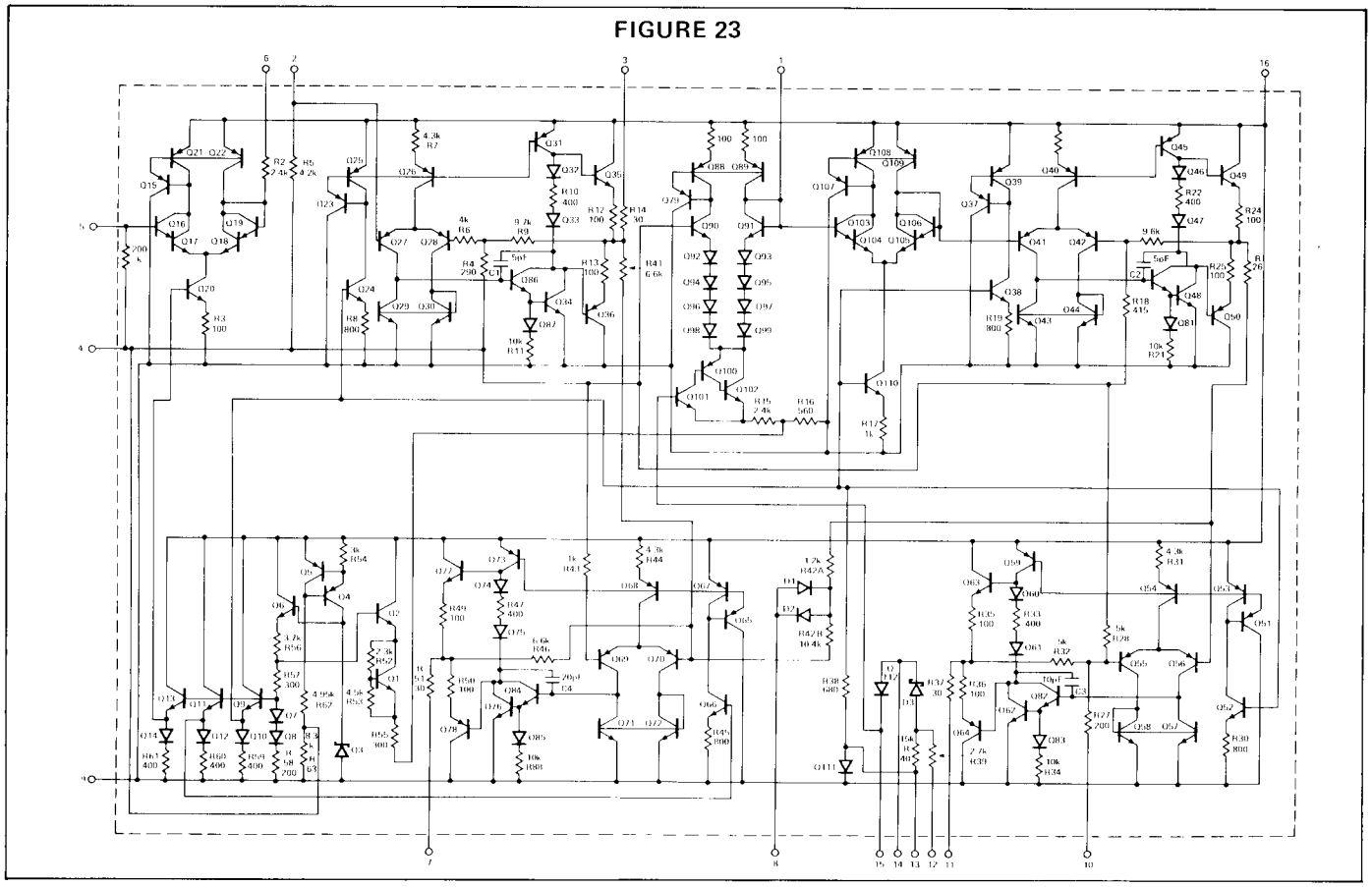
Output level of processor in record mode for constant input level.

i/P dB → / F Hz ↓	10	15	20	25	30	35	40
100	10.0	15.0	20.0	25.0	30.0	35.0	39.8
140	9.9	14.8	19.9	24.8	29.9	34.8	39.9
200	9.7	14.5	19.5	24.5	29.5	34.8	39.5
300	9.4	13.9	18.8	23.7	28.7	33.7	38.8
400	–	–	18.1	22.9	27.9	32.8	37.9
500	9.2	13.3	17.5	22.2	27.1	32.0	37.1
600	–	–	–	21.4	26.3	31.2	36.3
700	9.1	13.0	16.9	20.8	25.7	31.0	35.6
800	–	–	–	20.2	25.0	29.8	35.0
900	–	–	–	–	24.4	29.3	34.4
1k	9.1	12.8	15.8	19.4	24.0	28.8	33.8
1.2k	–	–	–	–	23.2	29.0	32.4
1.4k	9.2	12.8	15.6	18.5	22.6	27.4	32.4
2k	9.2	12.9	15.8	18.1	21.6	26.2	31.1
3k	9.2	13.1	16.2	18.5	21.2	25.4	30.3
5k	9.1	13.3	16.9	19.7	21.8	25.0	29.8
7k	9.0	13.4	17.2	20.3	22.7	25.3	29.7
10k	9.0	13.4	17.4	20.8	23.5	26.0	29.7
14k	8.9	13.3	17.3	21.0	24.0	26.6	29.8
20k	8.8	13.2	17.3	21.1	24.3	27.1	30.2

All dB figures are NEGATIVE (−) unless marked. 0dB = Dolby Level.

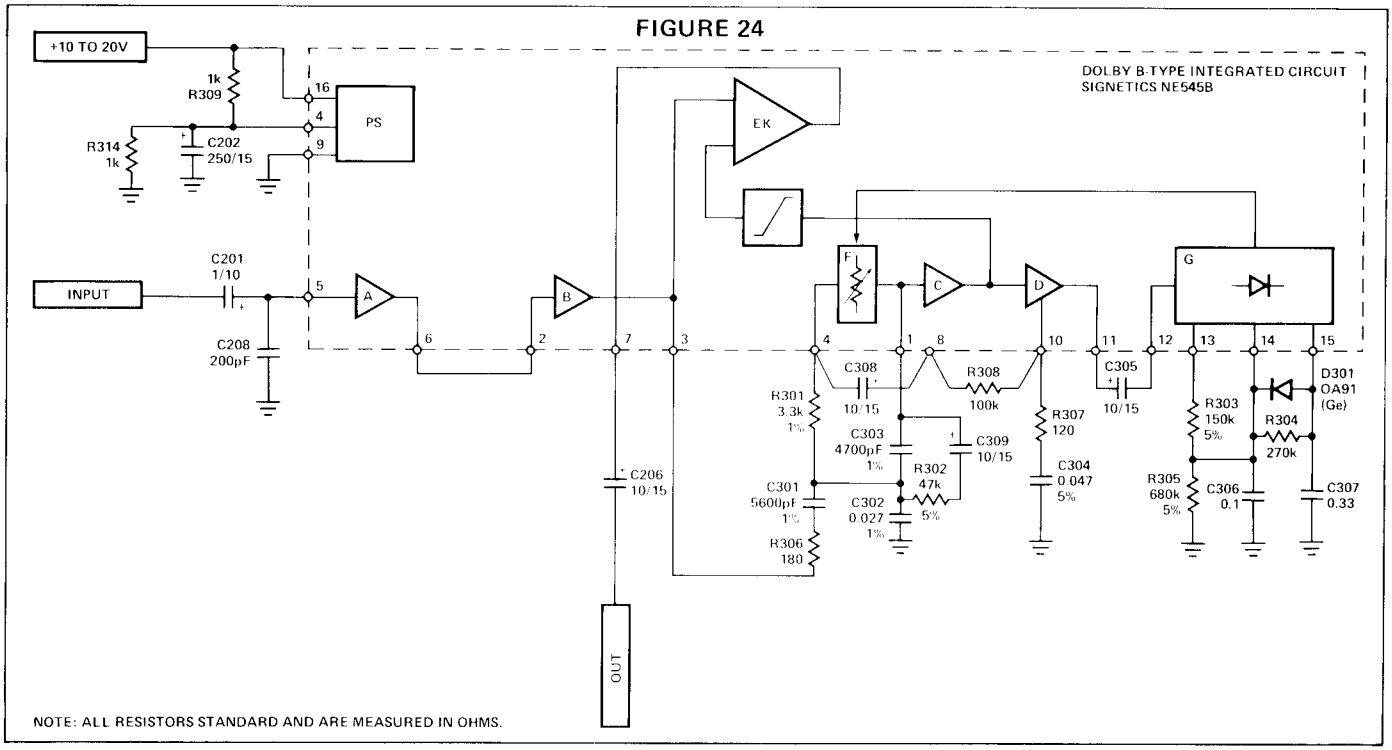
SCHEMATIC DIAGRAM

FIGURE 23



NE545B TEST CIRCUIT

FIGURE 24



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

NOTE:

A unique phenomenon may be observed in the rapid testing of the NE545. It is possible for C309 to become charged in a reverse polarity when the power to a device is switched on and off rapidly as might be encountered in a testing situation. This results in an increase in turn-on delay of the circuit. This condition can be prevented by placing a 150kΩ resistor in parallel with C309. This resistor is only required in the test circuit and not in the actual application in which the NE545 is used. If desired, the 150kΩ resistor can be used in the actual application without any degradation of the performance of the circuit.

NE545B TEST PROCEDURE

EQUIPMENT

1. Low distortion audio generator (H.P. 204D)
2. RMS Voltmeter (H.P. 400E)

Connect audio generator to the input of the test jig (Fig. 24). Adjust the input level to obtain 0dB (580mV) at pin 3 of the IC. Perform spot frequency measurement at the output (pin 7) of the IC. All readings should fall within ±2dB with respect to the standard recording data as shown in the Processor Characteristics Analysis Form. Optionally, rather than checking at spot frequencies, the entire frequency spectrum can be checked using a sweep generator and recorder.

INTRODUCTION

The Dolby B-type noise reduction system is designed for the reduction of hiss in consumer products. Employing techniques similar to those used in the wideband Dolby Laboratories A-type professional noise reduction equipment, the B-type system retains the advantage of inaudible action, good matching, and low distortion.

The B-type noise reduction system operates by boosting low-level high-frequency signals in the encode mode and attenuating the same signals in a complementary manner in the decode mode. During the latter process, noise in the treated frequency range is also attenuated.

In applying noise reduction to consumer tape products and FM receivers, it is necessary to appreciate that the full subjective improvement offered by a 10dB reduction in hiss can be obtained only if the other performance parameters of the system are of a comparable standard. The hum level, in particular, must be reduced to a lower value than is acceptable with normal hiss levels.

The Signetics NE545B Dolby-B Noise Processor can be used in three basic noise reduction circuits — encoders, decoders, and switchable processors which will operate in either mode.

CIRCUIT OPERATION

The operation of the noise reduction system will be described with reference to Figure 25, which is a block diagram of the encode and decode processor.

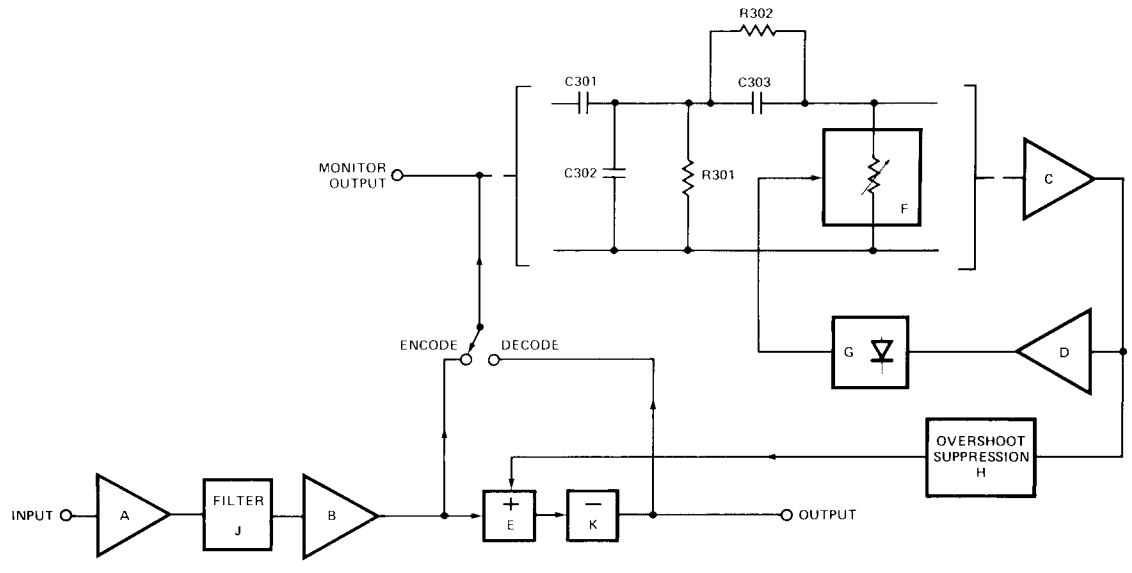
Referring to Figure 25, signals enter the encoder via amplifier A and pass to a low-pass filter J which attenuates all unwanted frequencies, such as tape recorder bias or FM multiplex signals, to a level of less than −45dB. If such spurious signals are above the threshold of the compressor, the full 10dB of low level pre-emphasis will not be obtained.

The signal at the output of amplifier B is split into two paths, one, known as the main path, provides an unaltered signal component directly to the output via adder E, while the other, known as the side chain, controls the dynamic characteristics of the processor.

The side chain contains a high-pass dynamic filter comprising capacitors C301, C302, C303 and resistors R301, R302 and the controlled resistance F. At low signal levels F has a high value and the first part of the filter (i.e. C301, C302, and R301) then controls the response of the side chain.

The output of the filter is amplified by amplifier C and the resulting noise reduction signal is added to the main signal in adder E. The low-level gain of the side-chain is such that the overall output is increased by 10dB at 5kHz when the noise reduction signal is added.

FIGURE 25
ENCODE-DECODE BLOCK DIAGRAM



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

CIRCUIT OPERATION (Con't.)

The side chain output is amplified further by D, and then rectified and smoothed by a non-linear integrator (block G). The resulting dc control signal is fed back to vary resistance F. When this control voltage exceeds a threshold value, the resistance of F falls, causing the turnover frequency of the second part of the filter (R302, C303, and F) to increase, thereby attenuating low and medium frequency signals in the side chain. With increasing input levels, the side chain signal becomes a decreasing proportion of the main signal, producing the transfer characteristics plotted in Figure 17. At 0dB the side chain signal is very small compared with the main signal, so that the signal is substantially unchanged by the added component.

The control circuit uses a non-linear smoothing scheme to avoid the generation of modulation products while providing fast response under transient conditions. For small changes in signal level, the charge and discharge time-constants are of the order of 100ms, but for sudden increases in signal level, the attach time is reduced to about 2ms. To avoid overshoots in the output during this interval, the side chain includes overshoot suppressor H, which operates only under extreme transient conditions during which the side chain is re-establishing its steady-state operating point. Thus, for a very short period, the encoded output consists of a large pure signal (via the direct path) and a small clipped component (via the side chain). Under steady state conditions the clipper H is inoperative.

For decoding, essentially the same circuitry is used, but in this case the side chain forms part of a negative feedback loop in which the noise reduction signal is subtracted from (instead of added to) the main path signal.

The decoder characteristics are therefore complementary to the encoder characteristics. Referring to Figure 25, which shows the decoder, the inverter K inverts the phase of the signal feeding the side chain relative to that in the encoder.

STANDARDIZATION OF LEVELS

For close matching, the two processors of a complete chain must operate under the same conditions. This means that the audio channel (tape recorder, broadcast transmitter-receiver path, etc.) between encoder and decoder must have a flat frequency response and a fixed gain, such that the signal voltage in the decode processor is the same (within 2dB) as that in the encode processor. The requirement for interchangeability of recordings and equipment imposes a further condition. The signal levels in the noise reduction system must be related to levels in the intervening channel in a fixed and internationally standardized manner.

In order to relate the various voltage levels and flux levels used in the complete recording or transmission chain, the concept of Dolby Level is employed. Dolby Level bears a fixed amplitude relationship firstly to the noise reduction compression and expansion parameters, and secondly to conditions in the chain between processors. It corresponds with a flux level in open reel tapes of 185nWb/m, a flux level on cassettes of 200nWb/m, a modulation deviation on FM transmissions of ±37.5kHz, and a voltage level at the output of the Dolby B-type processors of 580mV rms.

MATCHING AND MISMATCHING

Two processor units in a correctly manufactured and aligned chain can match at all frequencies of interest and all levels to within about ±1dB.

Mismatching can occur from a number of causes. Most commonly, the signal channel between encoder and decoder may not be correctly adjusted, either on a wideband basis (i.e. gain error) or at high frequencies only (frequency response error); the results of gain errors are shown in Figure 18.

Other possible errors arise from use of out of tolerance components.

SYSTEM REQUIREMENTS

Figure 32 illustrates the basic block diagram of a Dolby type noise reduction system as applied to a typical record-playback chain. The configurations employed for encoding and decoding are very similar, and can be regarded as the same circuit switched to operate in either mode.

Figure 25 shows the detailed block diagram of a practical circuit for incorporation in, for example, a consumer tape recorder. Some of the input, output and other interfacing characteristics of a practical circuit can be arbitrarily decided, but it is sensible to design so that the circuit may most economically be incorporated in consumer equipment. Hence, for example, input and output levels and impedances should permit the designer of a recorder to dispense with additional amplifiers. However, it is important that the input circuitry should not degrade the potential noise performance of the rest of the equipment. For this reason a compromise line input sensitivity of 30mV is employed; this will accommodate all international requirements except those of the DIN input stage.

The features of an overall system may then be listed:

Input	sufficient sensitivity to be used directly as input of consumer equipment, i.e. 30mV approximately into a minimum of 50 kohms.
Output	sufficient level to be used directly as output of consumer equipment, including meeting DIN specifications, i.e. 0.5–1.0 volts from a low impedance.
Distortion	less than that introduced by associated tape or FM equipment, e.g. 0.2% total harmonic distortion over low and middle frequencies up to perhaps 10dB above reference level, with some rise permissible at high frequencies and levels.
Noise	less than that introduced by associated tape or FM equipment, e.g. signal to noise ratio of at least 60dB.

DESIGN PHILOSOPHY

The requirements described above were met by the discrete component circuit already in extensive use at the time of the beginning of the integrated circuit development programme.

However, it is obvious that from the hardware manufacturer's viewpoint the introduction of a noise reduction system of such sophistication involves extra complexity during assembly and particularly during testing, when care and accuracy are required in making two pre-set alignment adjustments.

Therefore primary design considerations for the Dolby B-type IC were compatibility with the existing discrete component processor and elimination of the internal alignment procedures.

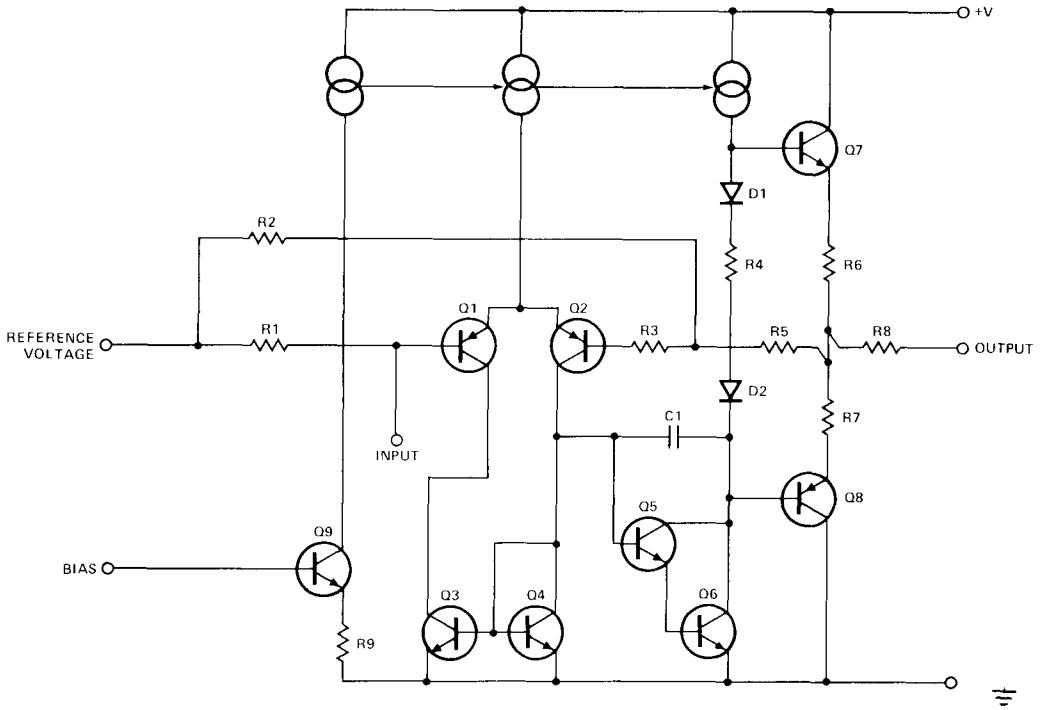
Once the feasibility of an IC processor had been established, it seemed reasonable to aim for a design whose interfacing parameters (input and output levels and impedances, switch requirements, close tolerance components, etc.) were similar to those of the existing discrete component circuit, so that those licensees who wanted to use the new integrated circuit could transfer to it with a minimum of design changes.

CIRCUIT DESCRIPTION

Figure 33 shows the block diagram of the IC with all functional block lettering the same as on Figure 25. The IC includes four identical operational amplifiers "B, C, D, and EK", two buffer amplifiers, a variable resistor, a rectifier system and a reference bias supply.

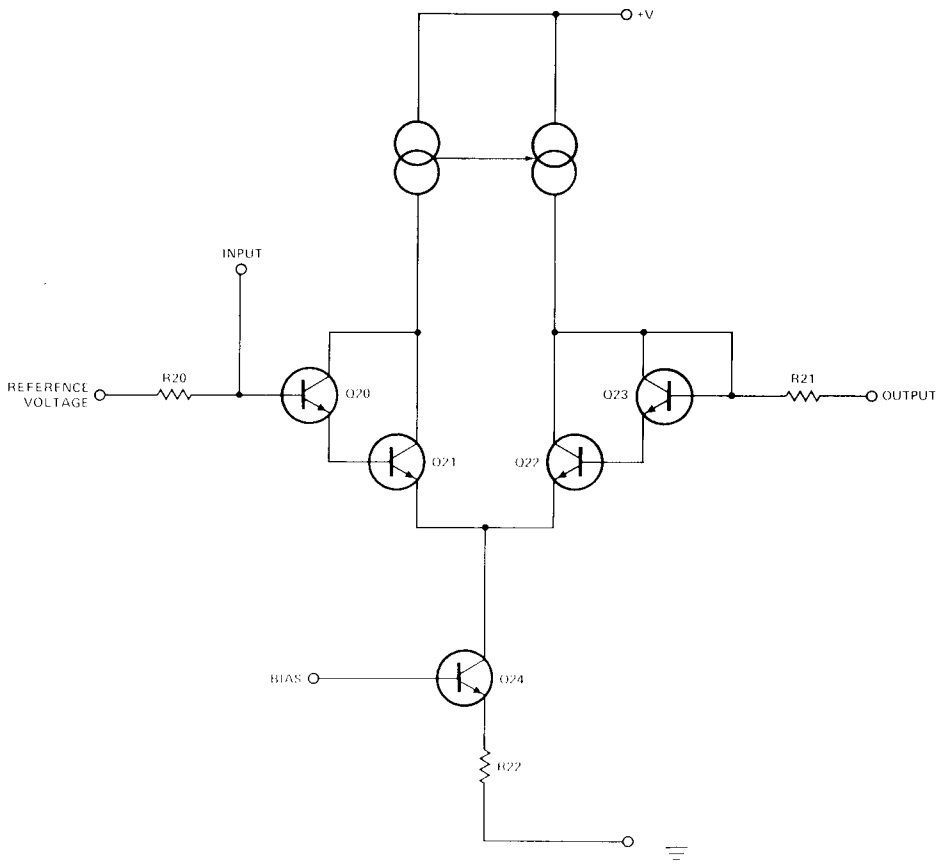
Choosing an operational amplifier design for the gain blocks has the advantage of providing a minimum of offset for DC coupling, a large output swing and a low output impedance. Figure 26 shows the basic circuit of the amplifier. The input consists of a differential PNP transistor pair Q_1, Q_2 which drives a Darlington stage Q_5, Q_6 followed by a class AB output stage Q_7, Q_8. Frequency compensation, necessary in all two-stage amplifiers for stable closed loop operation, is provided by capacitor C_1. Resistors R_4, R_6, R_7, set the quiescent current in the output stage, while R_8 limits the short circuit current and isolates the output from capacitive loads, which otherwise might cause oscillation due to excessive phase shift at high frequencies. The closed-loop gain of each amplifier is determined by internal resistors. The output swing and distortion characteristics of the amplifiers are shown in Figures 6 and 10.

FIGURE 26
BASIC OPERATIONAL AMPLIFIER



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

FIGURE 27
IMPEDANCE CONVERTER



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

CIRCUIT DESCRIPTION (Con't.)

Amplifier 'A' (Figure 27) is a unity gain impedance converter, providing high input and a given output impedance. A Darlington configuration is used for minimum bias current, keeping the output offset with respect to the reference voltage to a minimum. R_{21} gives the appropriate source impedance for the external low pass filter required to eliminate supersonic signals originating from FM tuners or from the bias and erase oscillators of tape recorders.

One of the most challenging aspects of the IC design was the development of a variable resistor (block F) with a wide dynamic range and a resistance versus control voltage law similar to that of the field effect transistor employed in the discrete component circuit.

The drain source conductance G_{DS} of a field effect transistor operating as a variable resistor is given by

$$G_{DS} = \frac{2\ I_{DSS}}{V_p^2} X\ [(V_{GS} - \frac{V_{DS}}{2}) - V_p]$$

where I_{DSS} is drain saturation current, V_p is gate pinch-off voltage, V_{GS} is gate-source bias, V_{DS} is drain-source voltage.

Provided the signal level applied to the device is small, G_{DS} is therefore a linear function of the gate-source voltage.

For a forward biased junction, the slope resistance R_J is given by

$$R_J = \frac{kT}{qI}$$

where k is Boltzmann's constant, T is absolute temperature, q is electronic charge, and I is forward current through junction.

Hence the slope conductance of the junction G_J is a linear function of the forward current, and it is possible to match the FET.

The chosen variable resistor circuit is shown in its basic form in Figure 28. By varying the current through the differential pair Q_1, Q_2 with the current sources 1 and 2, the input resistance at point 3 changes and its value is approximately

$$2\ X \frac{26\ X\ 10^{-3}}{I}\ \text{ohms}$$

at room temperature.

FIGURE 28. BASIC VARIABLE RESISTOR

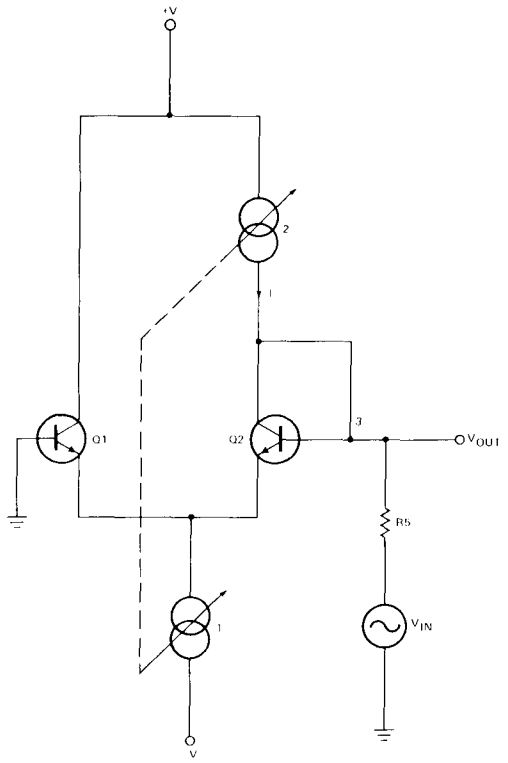
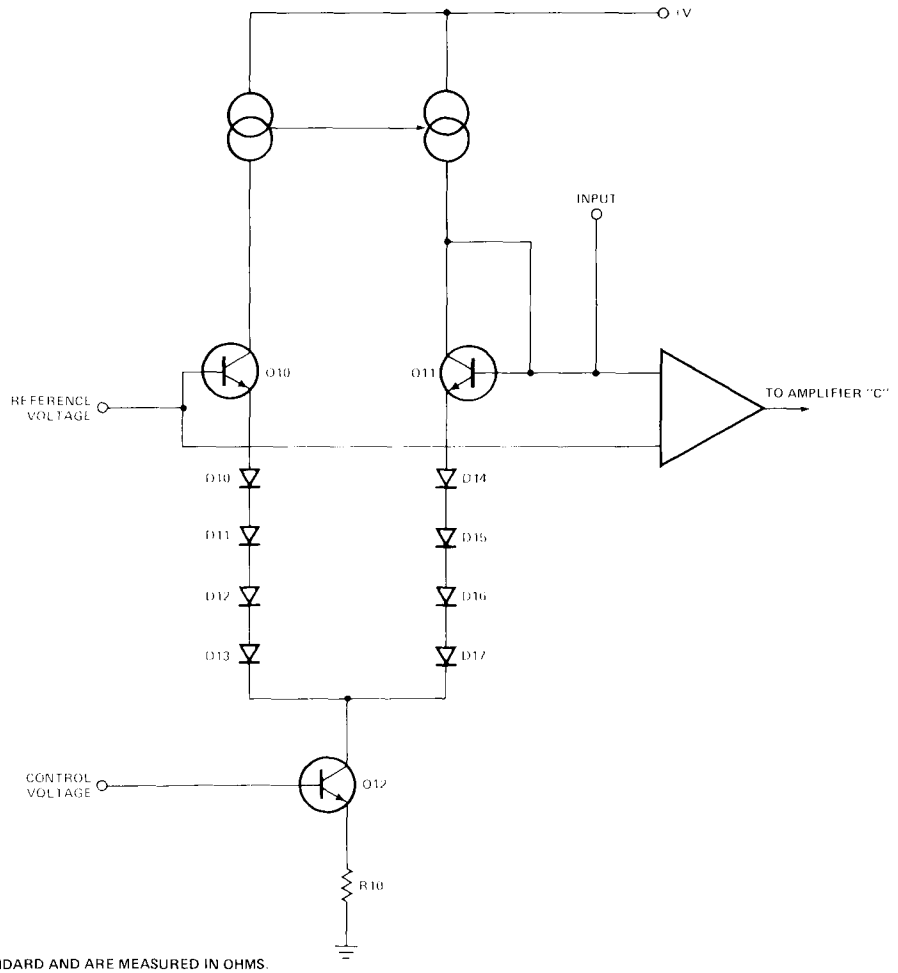


FIGURE 29. ACTUAL VARIABLE RESISTOR



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

CIRCUIT DESCRIPTION (Con't.)

In Figure 29 this principle has been transformed into a circuit as used in the IC. Additional diodes are inserted in the emitters of the differential pair in order to have a more manageable current range for the current source. The matching of the FET curve with the new circuit is shown in Figure 30. Since the variable resistance is a feedback amplifier, very little resistance modulation takes place; this is shown in a linearity graph (Figure 31) where THD is plotted against the input signal. For minimum loading of the variable resistance circuit, a Darlington buffer amplifier is used to drive amplifier "C".

FIGURE 30
RELATIVE CONTROL VOLTAGE
VERSUS RESISTANCE

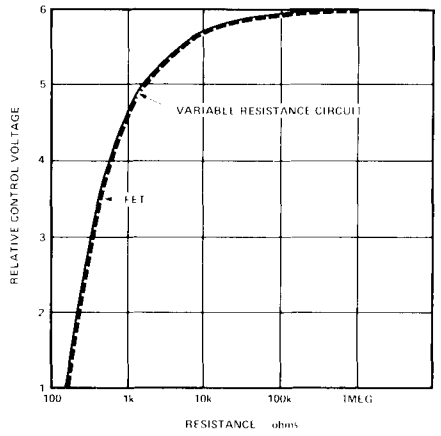
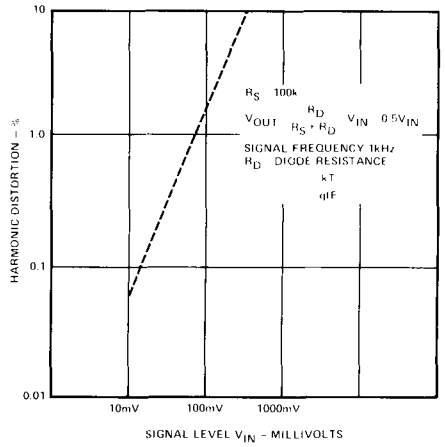


FIGURE 31
HARMONIC DISTORTION
VERSUS SIGNAL LEVEL



One important feature of the Dolby noise reduction system is that it is possible to substantially eliminate the overshoots which are normally associated with a compressor, and which give rise to transient distortion in the recording or transmission medium with consequent incorrect expansion (1).

In order to generate sufficient signal to operate the overshoot suppressor II, the noise reduction signal level is raised in amplifier C. The suppressor itself consists of a simple diode clipper.

The control amplifier "D" has a frequency dependent response determined by an external resistor and capacitor, and drives the rectifier section G via an AC coupling.

The rectifier of the discrete component circuit employs a germanium diode, and the IC had to reproduce closely its threshold characteristics. Prolonged development work showed that good matching could be obtained by the use of a Schottky barrier diode. The smoothing of the control signal is performed by a two stage integration circuit with a level dependent charging rate, providing rapid attack under conditions when the overshoot suppressor might operate, and more gradual gain variation under less stringent conditions. External components provide the necessary time constants.

Bias and reference voltages for the individual sections are generated by the internal regulated power supply. Each section has its own bias supply to insure good isolation.

CONCLUSIONS

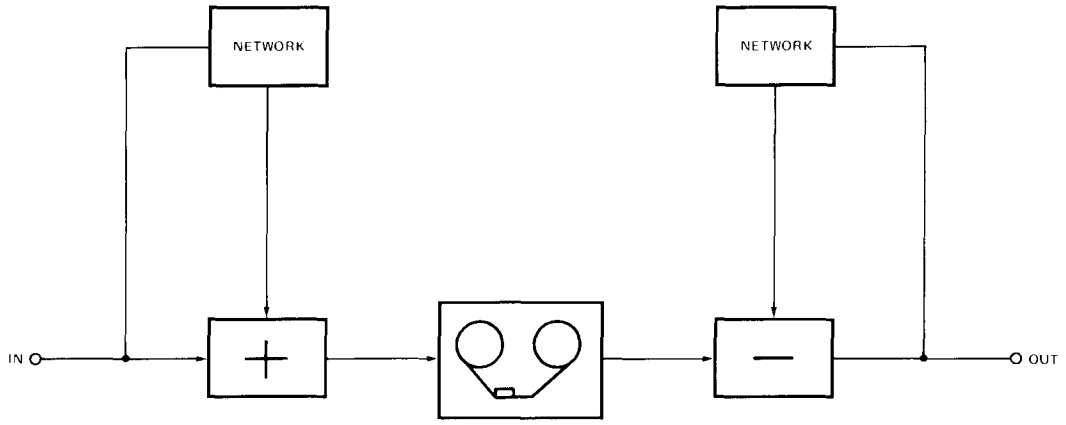
The device provides the desirable interfacing conditions for most economical incorporation in consumer equipment, so that, for example, the only additional electronics needed to complete one channel of a cassette recorder are a bias oscillator, a recording amplifier (one transistor), and a microphone and head amplifier (two transistors). The use of the IC permits the elimination of about 50 components/channel, with a saving of approximately 100 soldered joints. In large quantity production the IC provides worthwhile reductions in overall component cost and in assembly and testing times.

Integrated circuit processors meet the originally stated requirements comfortably, and the standard Dolby B-type characteristics (originally those of the discrete component circuit) are met typically within a tolerance of 1dB.

REFERENCES

1. R.M. Dolby, "An audio noise reduction system", Journal of the Audio Engineering Society, Vol. 15.4 (1967).
2. R.M. Dolby, "A noise reduction system for consumer tape recording". Presented at Audio Eng. Soc. 1970 Convention in New York.
3. R. Berkovitz and K.J. Gundry, "Dolby B-type noise reduction system". Audio, Sept./Oct. 1973.
4. D.P. Robinson, "Production of Dolby B-type cassettes", Journal of the Audio Engineering Society, Vol. 20.10 (1972).
5. D.P. Robinson, "Dolby B-type noise reduction for FM broadcasts", Journal of the Audio Engineering Society, Vol. 21.5 (1973).
6. R.M. Dolby, "Optimum use of noise reduction in FM broadcasting", Journal of the Audio Engineering Society, Vol. 21.5 (1973).

FIGURE 32
BASIC SYSTEM BLOCK DIAGRAM



APPLICATION INFORMATION

In addition to the system and circuit description, there are some variations to the circuit connection which may be useful in some applications. All of these variations to the basic system are shown in Figure 39; however, they can be applied to any of the various basic system diagrams.

The switch-on delay of the circuit can be reduced by changing the input coupling capacitor (C201) from 1μF to 0.1μF

Switching noise can be eliminated by referencing all capacitors which have to be switched to their operating potentials via a high value resistor (R311, 312, 313). Under these conditions the capacitors will maintain their potentials in any switch position.

For an improvement in signal to noise of up to 6dB, the signal can be injected directly into pin 2 via an appropriate coupling capacitor. Should it be necessary to maintain the filter network, a low noise emitter follower stage will have to be added.

The 545 back-to-back frequency response can be improved by replacing the resistor R305 (680k) with a 1.5Meg Ohm potentiometer. This allows the user to minimize the frequency response to less than ±1dB. This control is set by introducing a 1kHz signal into pin 3 at a level of 58mV (−20dB Dolby level). Then adjust the potentiometer until output reaches as close as possible −15.8dB Dolby level at pin 7; this automatically optimizes the frequency response levels.

The following diagrams show the many system configurations in which the NE545B Dolby-B Noise Processor can be used.

Figure 33 Class I Switchable Processor With Multiplex Filter

Figure 34 Class II Encode Processor With Multiplex Filter

Figure 35 Class III Decode Processor With Bias Filter

Figure 36 Class IV Decode Processor With Multiplex Filter

Figure 37 Class V Decode Processor Without Filter

Figure 38 FM Decode Processor (Switchable)

Figure 39 Class I Processor Showing Circuit Variations

FIGURE 33. CLASS I SWITCHABLE PROCESSOR WITH MULTIPLEX FILTER

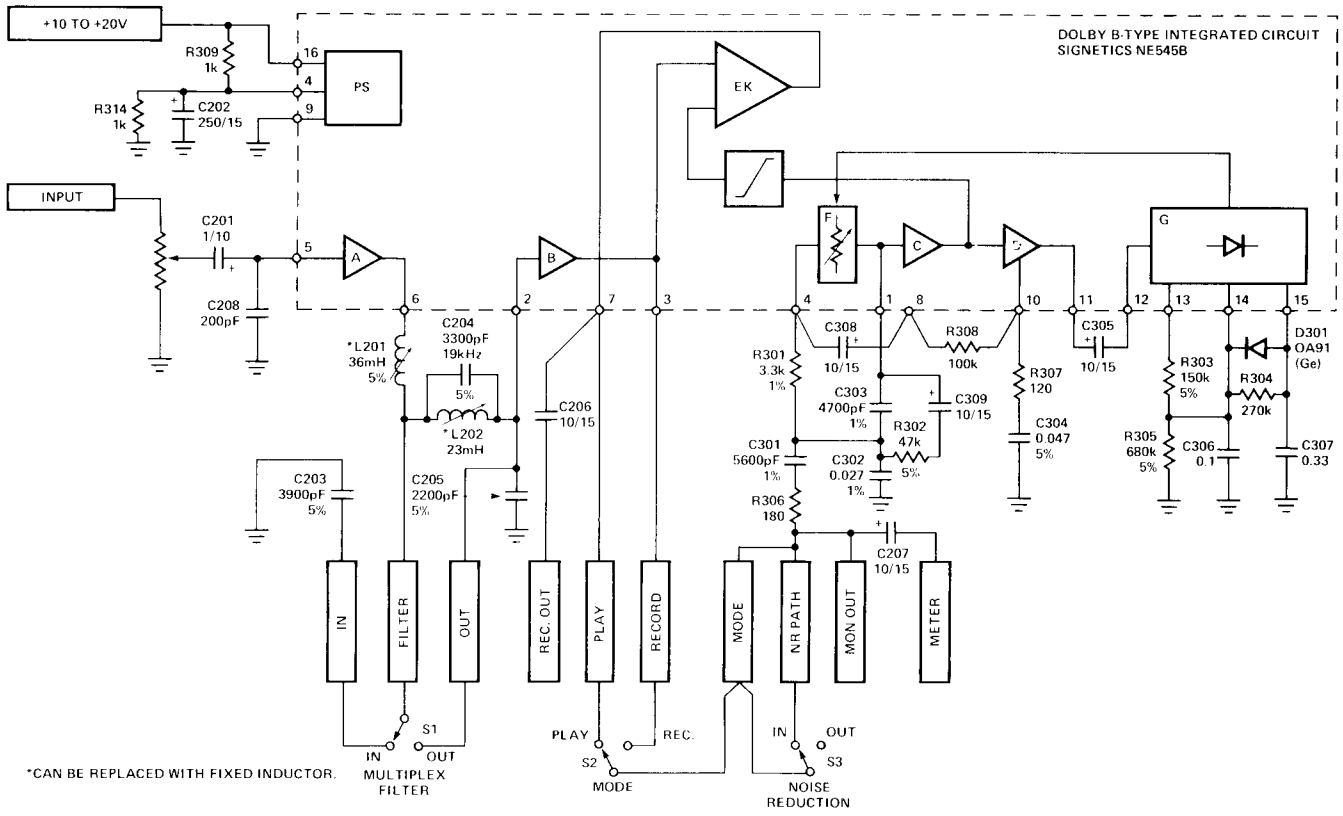
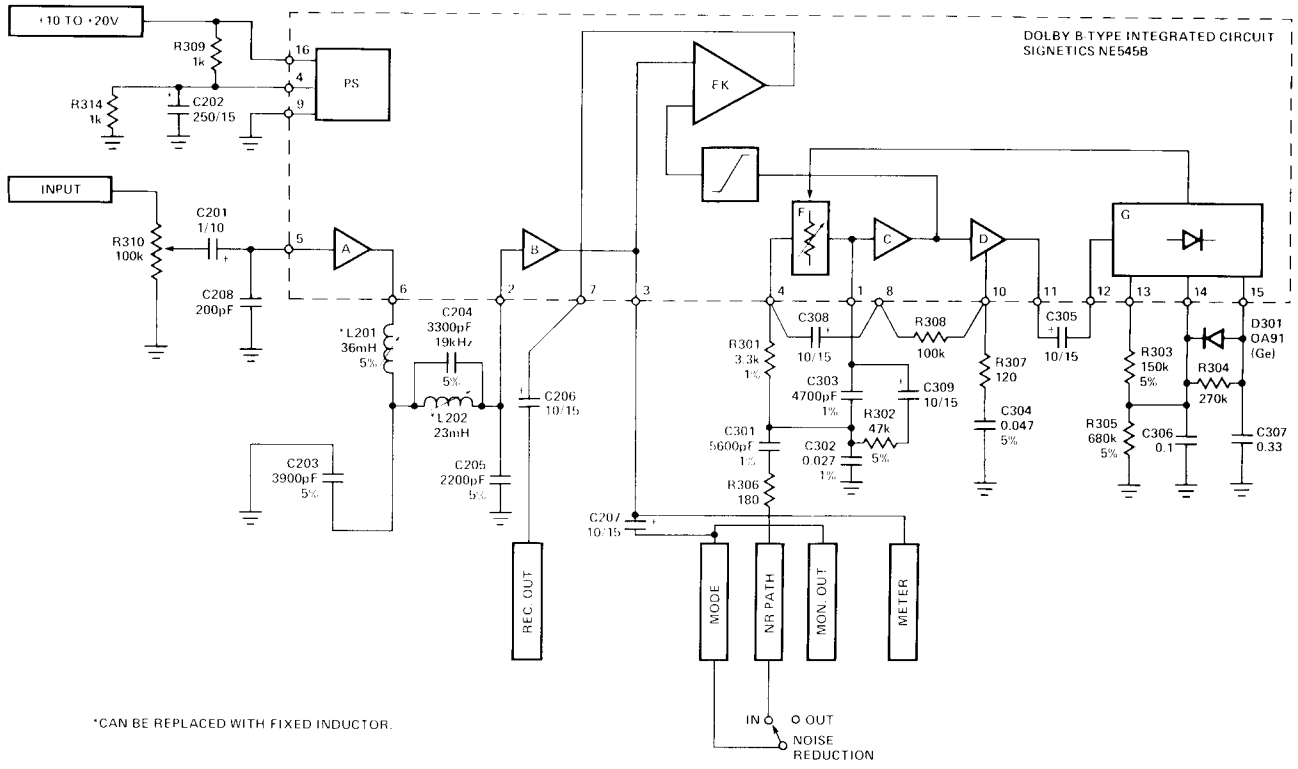


FIGURE 34. CLASS II ENCODE PROCESSOR WITH MULTIPLEX FILTER



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

FIGURE 35. CLASS III DECODE PROCESSOR WITH BIAS FILTER

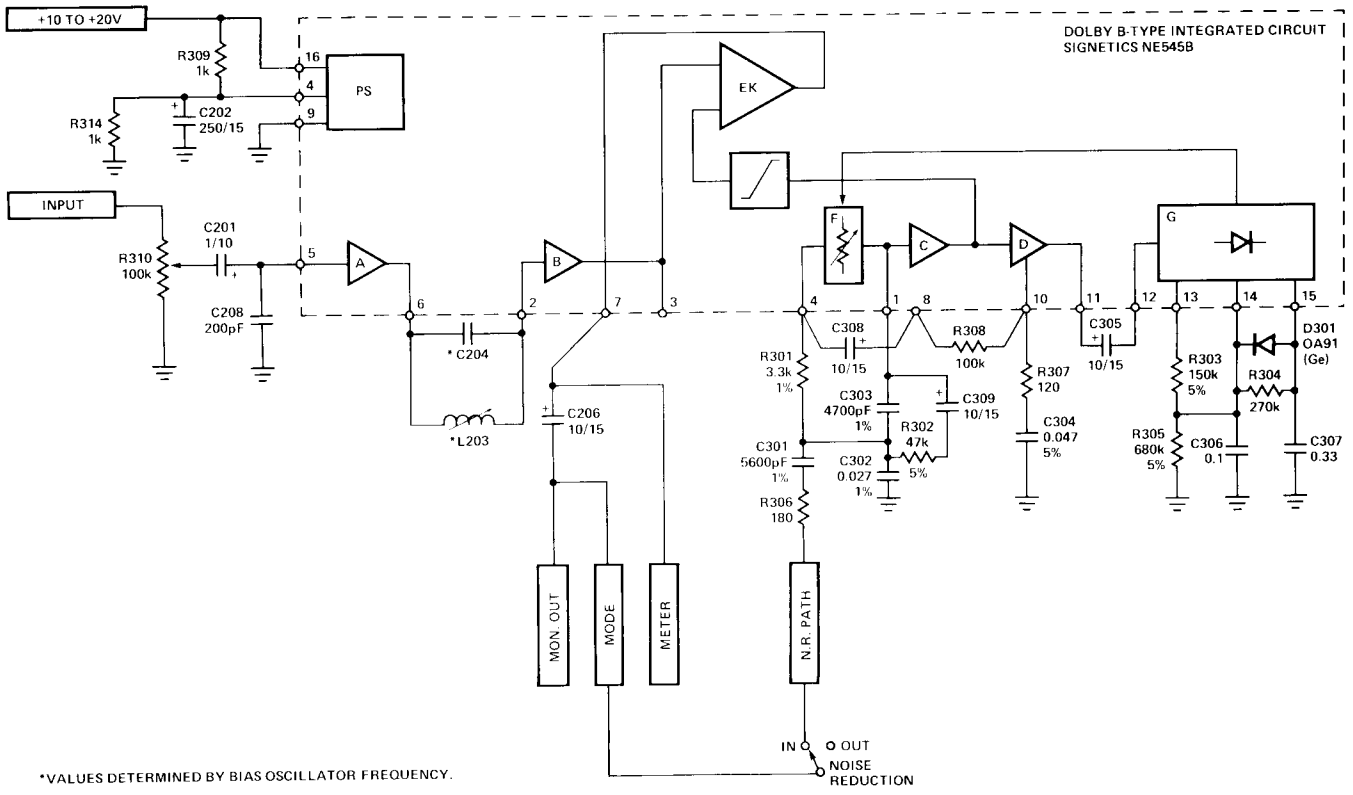
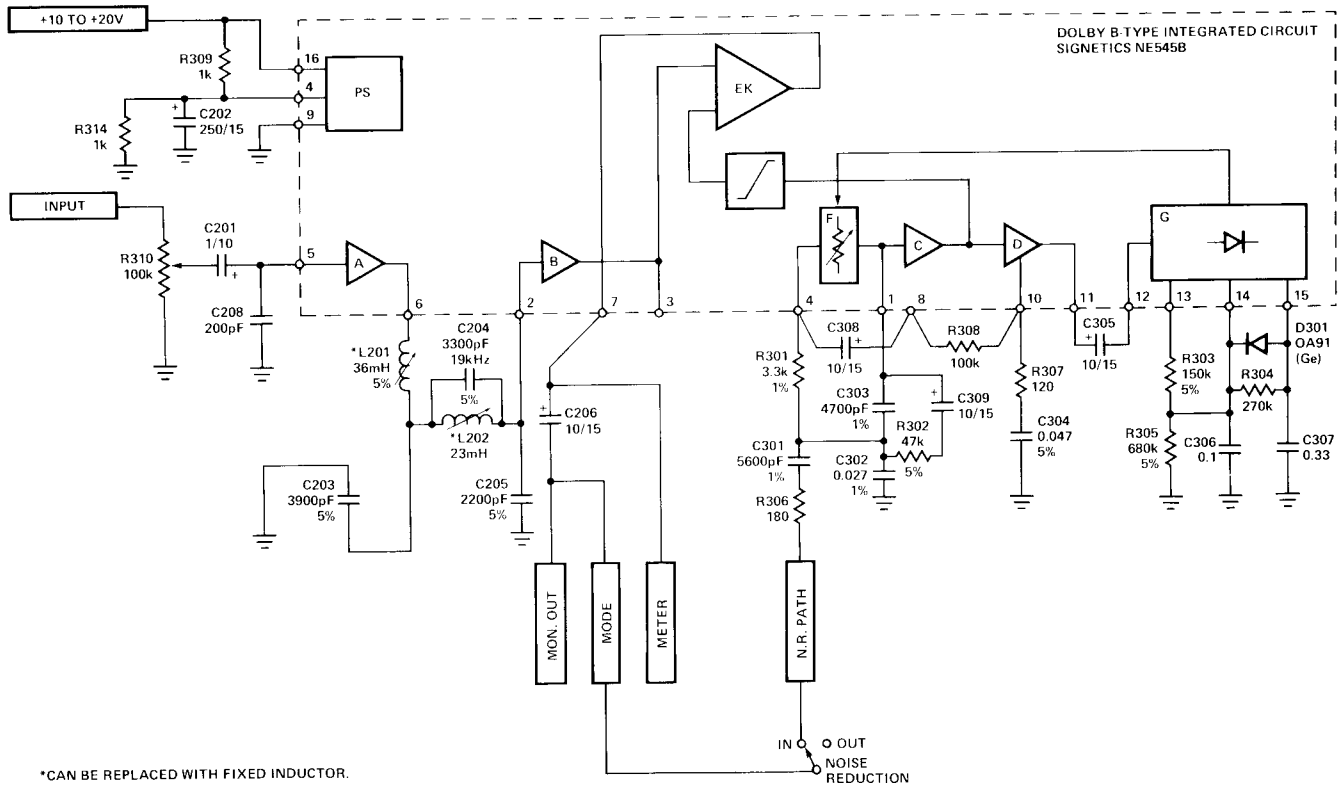


FIGURE 36. CLASS IV DECODE PROCESSOR WITH MULTIPLEX FILTER



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

FIGURE 37. CLASS V DECODE PROCESSOR WITHOUT FILTER

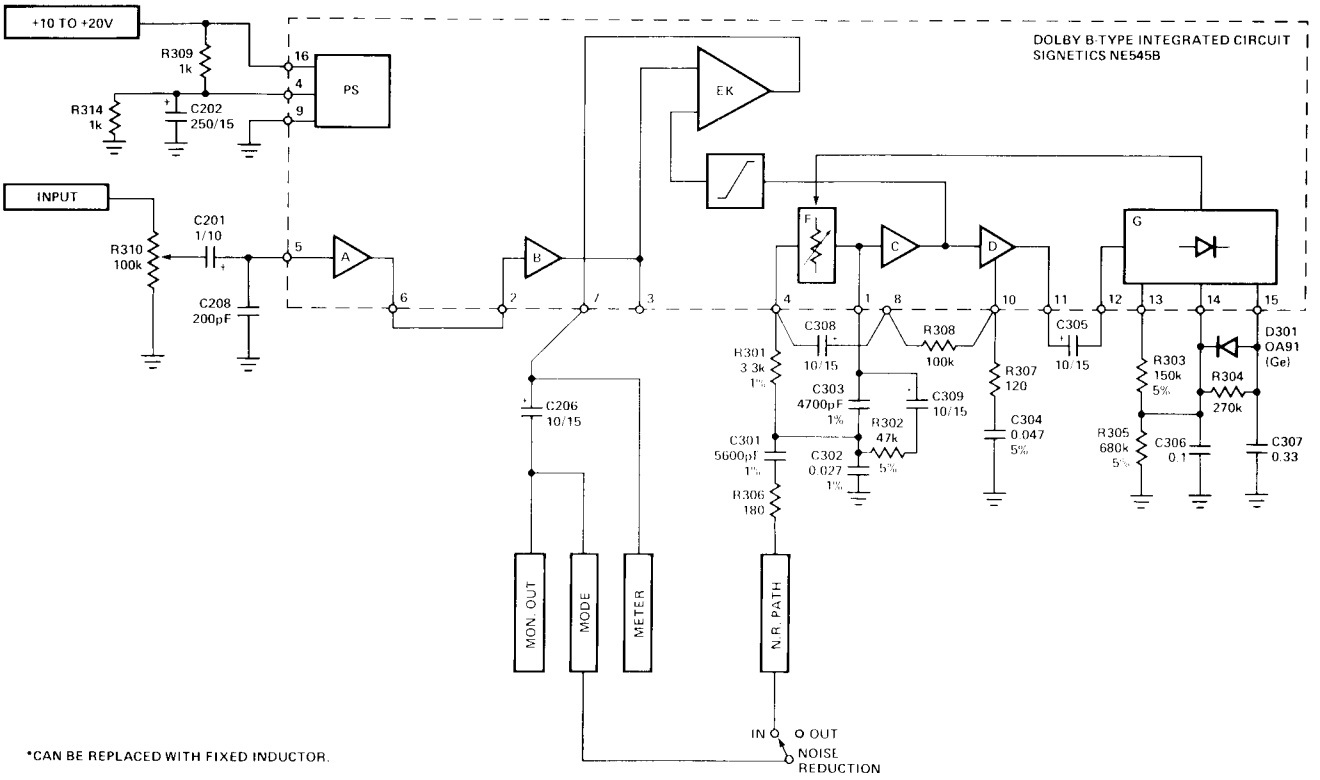
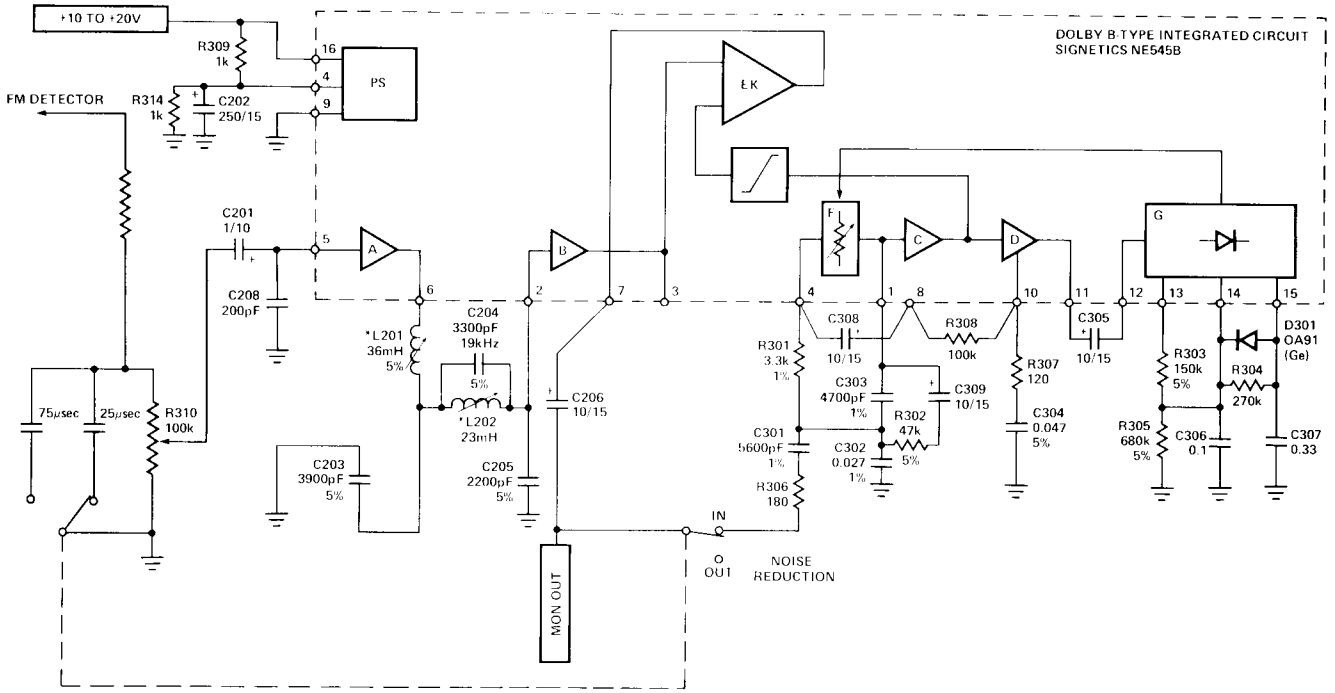
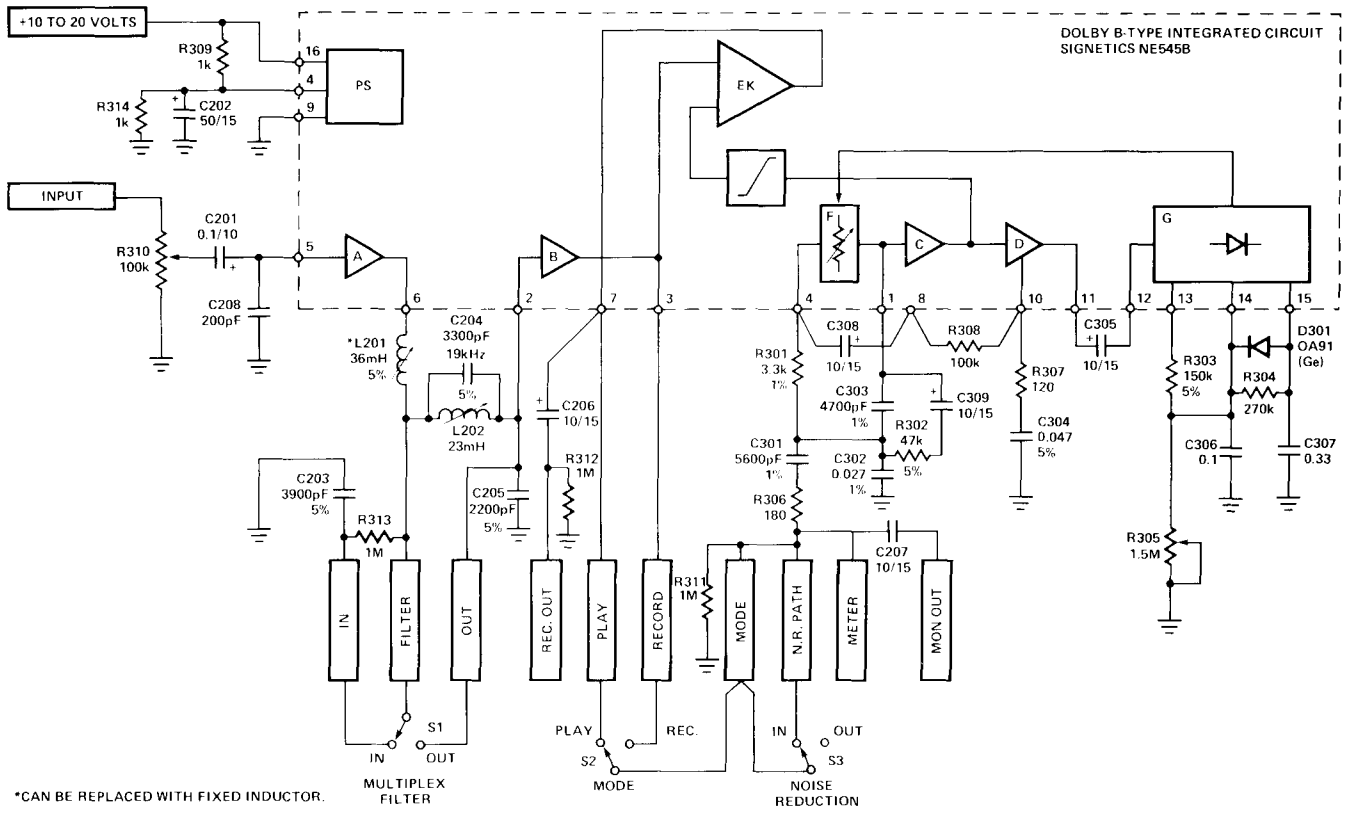


FIGURE 38. FM DECODE PROCESSOR (SWITCHABLE)

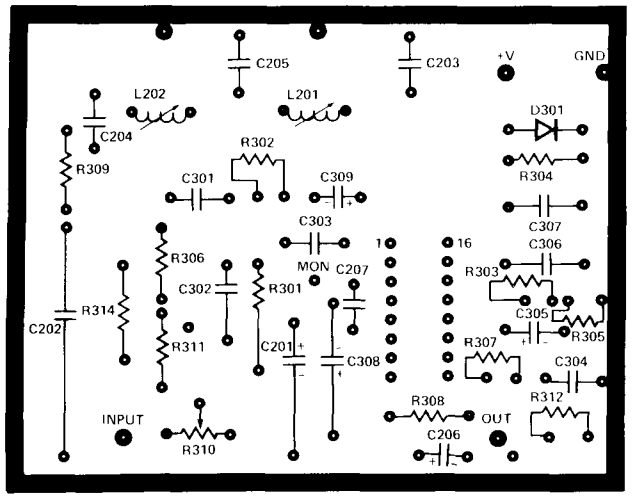


NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

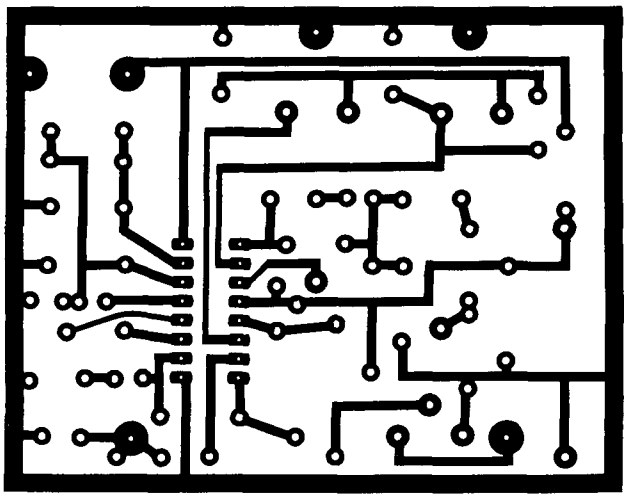
FIGURE 39. CLASS I PROCESSOR SHOWING CIRCUIT VARIATIONS



BOARD LAYOUT FOR DOLBY-B CLASS I PROCESSOR



TOP VIEW



BOTTOM VIEW

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

PARTS LIST FOR DOLBY-B CLASS I PROCESSOR

PART	VALUE	WATT	MAX. TOL. %	TYPE-PART NO.
R301	3.3kΩ	1/2	1	3321F RN60D
302	47kΩ	1/4	5	Carbon Comp
303	150kΩ	1/4	5	"
304	270kΩ	1/4	10	"
305	680kΩ	1/4	5	"
306	180Ω	1/4	10	"
307	120Ω	1/4	5	"
308	100k	1/4	10	"
309	1kΩ	1/4	10	"
310	100kΩ	1/4	5	R104B CTS Trimmer
311	1 Meg Ω	1/4	10	Carbon Comp
312	1 Meg Ω	1/4	10	"
314	1kΩ	1/4	10	"
C201	1μF 10V		10	Electrolytic
202	250μF 15V		10	"
203	3900pF		5	Mylar Elpac Z 1R 392J
204	3300pF		5	" Z 1R 332J
205	2200pF		5	" Z 1R 222J
206	10μF 15V		10	Electrolytic
208	200pF		20	Ceramic
C301	5600pF		1	Mylar Elpac Z 1R 562F
302	.027μF		1	" Z 1R 273F
303	4700pF		1	" Z 1R 472F
304	.047μF		5	" Z 1R 473J
305	10μF 15V		10	Electrolytic
306	.1μF		10	Mylar Elpac Z 1R 104K
307	.33μF		10	" Z 1R 334K
308	10μF 15V		10	Electrolytic
309	10μF 15V		10	"
L201	20-60MH		Adjustable	J.W. Miller 9063
202	15-40MH		Adjustable	J.W. Miller 9062
D301	Germanium OA91			IN34A, IN64A

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811 EAST ARQUES AVENUE ■ SUNNYVALE, CALIFORNIA ■ 94086
TEL: (408) 739-7700 ■ TWX: (910) 339-9283