COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4518B
HCC/HCF 4520B

DUAL UP-COUNTERS: HCC/HCF 4518B DUAL BCD UP-COUNTER
HCC/HCF 4520B DUAL BINARY UP-COUNTER

- MEDIUM-SPEED OPERATION - 6 MHz TYP. CLOCK FREQUENCY AT 10V
- POSITIVE - OR NEGATIVE - EDGE TRIGGERING
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- QUIESCENT CURRENT SPECIFIED TO 20V
- MAXIMUM INPUT CURRENT OF 1 μA AT 18V (FULL PACKAGE TEMPERATURE RANGE)
- 5V, 10V, AND 15V PARAMETRIC RATINGS

The **HCC 4518B/4520B** (extended temperature range) and **HCF 4518B/4520B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package. The **HCC/HCF 4518B** Dual BCD Up Counter and **HCC/HCF 4520B** Dual Binary Up Counter each consist of two identical, internally synchronous 4-stage counters. The counter stages are D-type flip-flops having interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition. For single-unit operation the Enable input is maintained "high" and the counter advances on each positive-going transition of the Clock. The counters are cleared by high levels on their Reset lines. The counter can be cascaded in the ripple mode by connecting Q4 to the enable input of the subsequent counter while the clock input of the latter is held low.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage	-0.5 to 20	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor		
	for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage
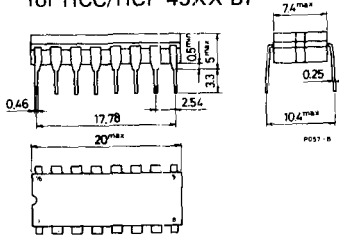
ORDERING NUMBERS:

HCC 45XX BD   for dual in-line ceramic package
HCC 45XX BF   for dual in-line ceramic package, frit seal
HCC 45XX BK   for ceramic flat package
HCF 45XX BE   for dual in-line plastic package
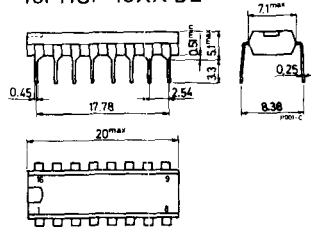HCF 45XX BF   for dual in-line ceramic package, frit seal

HCC/HCF 4518B
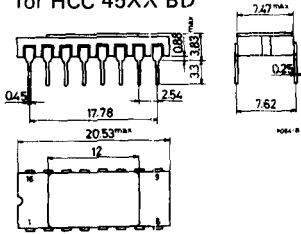# HCC/HCF 4520B

MECHANICAL DATA (dimensions in mm)

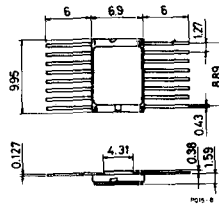Dual in-line ceramic package
for HCC/HCF 45XX BF
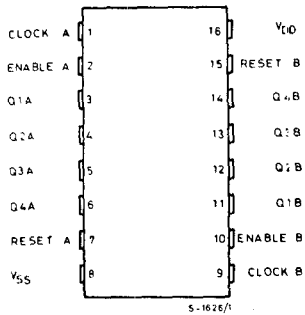
Dual in-line plastic package
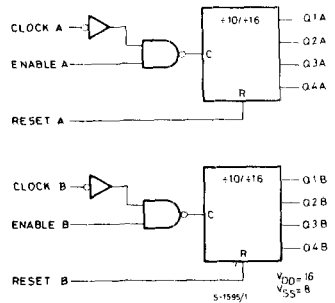for HCF 45XX BE

Dual in-line ceramic package
for HCC 45XX BD

Ceramic flat package
for HCC 45XX BK

CONNECTION DIAGRAM

CLOCK A	1	16	V_{DD}
ENABLE A	2	15	RESET B
Q1A	3	14	Q4B
Q2A	4	13	Q3B
Q3A	5	12	Q2B
Q4A	6	11	Q1B
RESET A	7	10	ENABLE B
V_{SS}	8	9	CLOCK B

S-1626/1

FUNCTIONAL DIAGRAM

CLOCK A
ENABLE A
+10/+16
C
Q1A
Q2A
Q3A
Q4A
R
RESET A

CLOCK B
ENABLE B
+10/+16
C
Q1B
Q2B
Q3B
Q4B
R
RESET B

V_{DD} = 16
V_{SS} = 8

S-1595/1

RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage	3 to 18	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: for **HCC** types	-55 to 125	°C
	for **HCF** types	-40 to 85	°C

428

LOGIC DIAGRAMS (for one of two identical counter)

Decade counter for 4518B
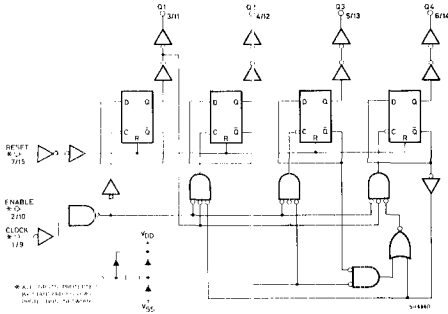
Binary counter for 4520B
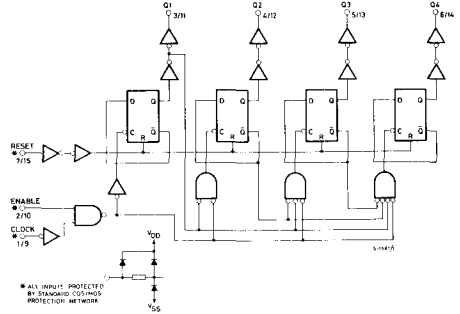
TRUTH TABLE

CLOCK	ENABLE	RESET	ACTION
⤴	1	0	Increment Counter
0	⤵	0	Increment Counter
⤵	X	0	No Change
X	⤴	0	No Change
⤴	0	0	No Change
1	⤵	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care   1 = High State   0 = Low State

TIMING DIAGRAM
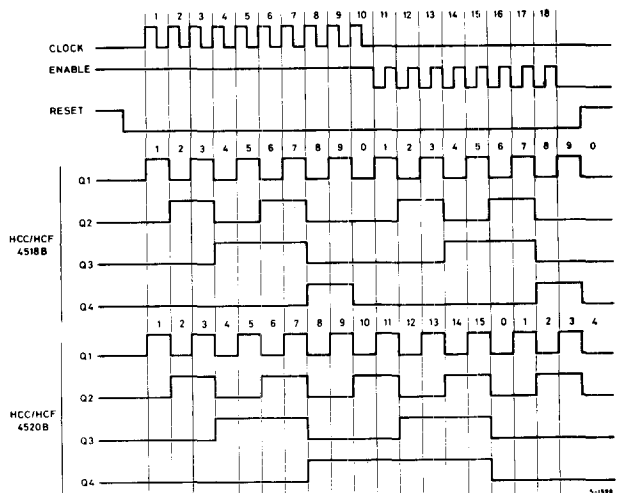
STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter		V_I (V)	V_O (V)	$\|I_O\|$ (µA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	Unit
I_L	Quiescent supply current	0/ 5			5		5		0.04	5		150	µA
		0/10			10		10		0.04	10		300	
		0/15			15		20		0.04	20		600	
		0/20			20		100		0.08	100		3000	
V_{OH}	Output high voltage	0/ 5		<1	5	4.95		4.95			4.95		V
		0/10		<1	10	9.95		9.95			9.95		
		0/15		<1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage		0.5/4.5	<1	5	3.5		3.5			3.5		V
			1/9	<1	10	7		7			7		
			1.5/13.5	<1	15	11		11			11		
V_{IL}	Input low voltage		4.5/0.5	<1	5		1.5			1.5		1.5	V
			9/1	<1	10		3			3		3	
			13.5/1.5	<1	15		4			4		4	
I_{OH}	Output drive current HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
		0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
	HCF types	0/ 5	2.5		5	-1.8		-1.6	-3.2		-1.3		
		0/ 5	4.6		5	-0.61		-0.51	-1		-0.42		
		0/10	9.5		10	-1.5		-1.3	-2.6		-1.1		
		0/15	13.5		15	-4		-3.4	-6.8		-2.8		
I_{OL}	Output sink current HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	HCF types	0/ 5	0.4		5	0.61		0.51	1		0.42		
		0/10	0.5		10	1.5		1.3	2.6		1.1		
		0/15	1.5		15	4		3.4	6.8		2.8		
I_{IH}, I_{IL}**	Input leakage current	0/18			18		±0.1		±10^{-5}	±0.1		± 1	µA
C_i**	Input capacitance								5	7.5			pF

* T_{Low} = $-55°C$ for **HCC** device; $-40°C$ for **HCF** device.
* T_{High} = $+125°C$ for **HCC** device; $+85°C$ for **HCF** device.
** Any input

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
2V min. with V_{DD} = 10V
2.5V min. with V_{DD} = 15V

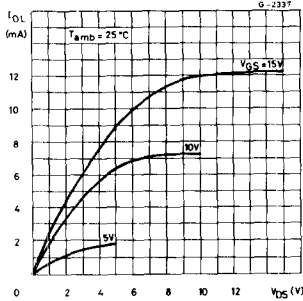# DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C, C_L= 50 pF, R_L= 200 kΩ, typical temperature coefficient for all V_{DD} values is 0.3%/°C, all input rise and fall times = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PLH}, t_{PHL}	Propagation delay time (Clock or Enable to output)	5		280	560	ns
		10		115	230	
		15		80	160	
t_{PLH}, t_{PHL}	Propagation delay time (Reset to output)	5		330	650	ns
		10		130	225	
		15		90	170	
t_{TLH}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_W	Clock pulse width	5	200	100		ns
		10	100	50		
		15	70	35		
t_W	Reset pulse width	5	250	125		ns
		10	110	55		
		15	80	40		
t_W	Enable pulse width	5	400	200		ns
		10	200	100		
		15	140	70		
t_r, t_f	Clock or enable rise and fall time	5			15	µs
		10			15	
		15			5	
f_{CL}	Maximum clock frequency	5	1, 5	3		MHz
		10	3	6		
		15	4	8		

Typical output low (sink) current characteristics

I_{OL} (mA)
$T_{amb} = 25°C$
$V_{GS} = 15V$
10V
5V
24 20 16 12 8 4
0 2 4 6 8 10 12 V_{DS}(V)
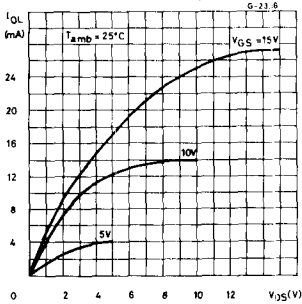
Minimum output low (sink) current characteristics

I_{OL} (mA)
$T_{amb} = 25°C$
$V_{GS} = 15V$
10V
5V
12 10 8 6 4 2
0 2 4 6 8 10 12 V_{DS} (V)

Typical output high (source) current characteristics

$-I_{OH}$ (mA)
$V_{GS} = -5V$
-10V
-15V
$T_{amb} = 25°C$
10 20 30
0 5 10 $-V_{DS}$ (V)
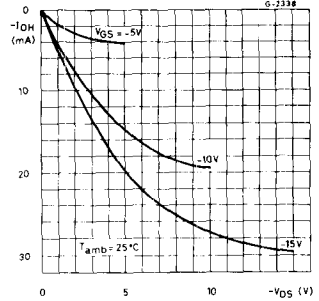
Minimum output high (source) current characteristics

$-I_{OH}$ (mA)
$V_{GS} = -5V$
-10V
-15V
$T_{amb} = 25°C$
5 10 15
0 5 10 $-V_{DS}$ (V)
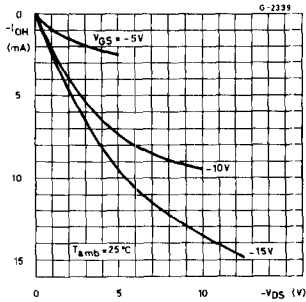
Typical propagation delay vs. load capacitance, reset to output

t_{PLH}
t_{PHL} (ns)
$T_{amb} = 25°C$
$V_{DD} = 5V$
10V
15V
320 280 240 200 160 120 80 40
0 10 20 30 40 50 60 70 80 C_L (pF)
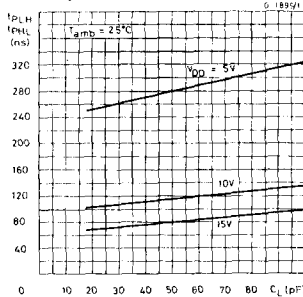
Typical propagation delay time vs. load capacitance, clock or enable to output

t_{PLH}
t_{PHL} (ns)
$V_{DD} = 5V$
$T_{amb} = 25°C$
10V
15V
320 280 240 200 160 120 80 40
0 10 20 30 40 50 60 70 80 C_L (pF)
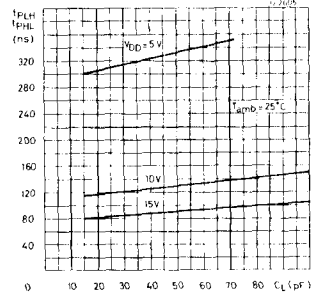
Typical transition time vs. load capacitance

t_{TLH}
t_{THL} (ns)
$T_{amb} = 25°C$
$V_{DD} = 5V$
10V
15V
160 140 120 100 80 60 40 20
0 10 20 30 40 50 60 70 80 C_L (pF)
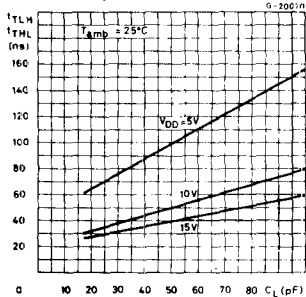
Typical maximum-clock frequency vs. supply voltage

f_{max} (MHz)
$T_{amb} = 25°C$
$C_L = 50pF$
15 10 5
0 5 10 15 V_{DD} (V)
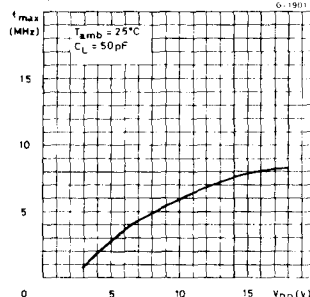
Typical power dissipation/counter vs. frequency

P_{tot} (μW)
$V_{DD} = 15V$ 10V 10V 5V
$T_{amb} = 25°C$
$C_L = 50pF$
$C_L = 15pF$
f (kHz)
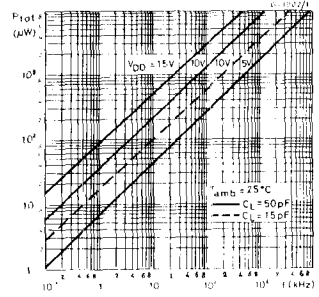
TEST CIRCUITS

Quiescent device current

V_DD

V_DD
INPUTS
V_SS

I_DD

V_SS

S-1992/1

Noise immunity

V_DD

INPUTS   OUTPUTS

V_IH

V_IL

DVM

NOTE :
TEST ANY COMBINATION
OF INPUTS

V_SS   S-2079/1

Input leakage current

V_DD

INPUTS

V_DD

1

V_SS

NOTE: MEASURE INPUTS
SEQUENTIALLY. TO BOTH
V_DD AND V_SS CONNECT
ALL UNUSED INPUTS TO
EITHER V_DD OR V_SS

V_SS

S-1994/1
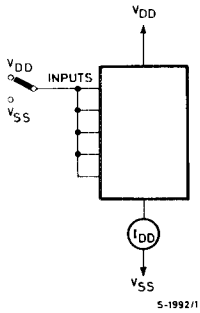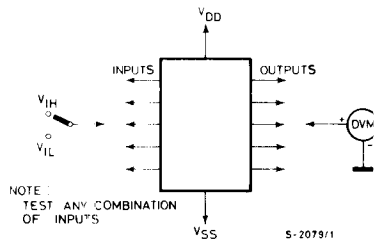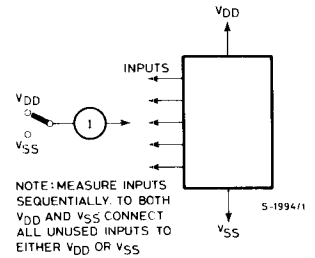
Dynamic power dissipation

V_DD

500 μF   I_D   0.01 μF
CERAMIC

PULSE
GENERATOR   C   Q1

Q2
C_L
Q3
C_L
E   Q4
C_L
R

t_r = t_f = 20ns   S-1599/1

V_SS
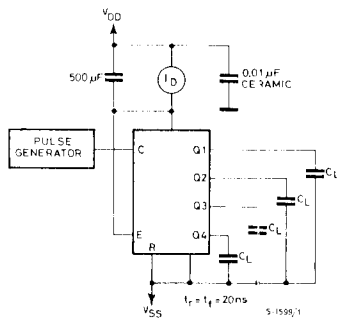
TYPICAL APPLICATIONS

Ripple cascading of four counters with positive-edge triggering

CLOCK
INPUT

V_DD

| 1 | 2 | 7 | | 9 | 10 | 15 | | 1 | 2 | 7 | | 9 | 10 | 15 |
CLOCK ENABLE RESET   CLOCK ENABLE RESET   CLOCK ENABLE RESET   CLOCK ENABLE RESET
A   A   A   B   B   B   A   A   A   B   B   B

Q1A Q2A Q3A Q4A   Q1B Q2B Q3B Q4B   Q1A Q2A Q3A Q4A   Q1B Q2B Q3B Q4B
3   4   5   6   11   12   13   14   3   4   5   6   11   12   13   14

HCC/HCF4518B-20B   HCC/HCF4518B-20B

S-1600/1
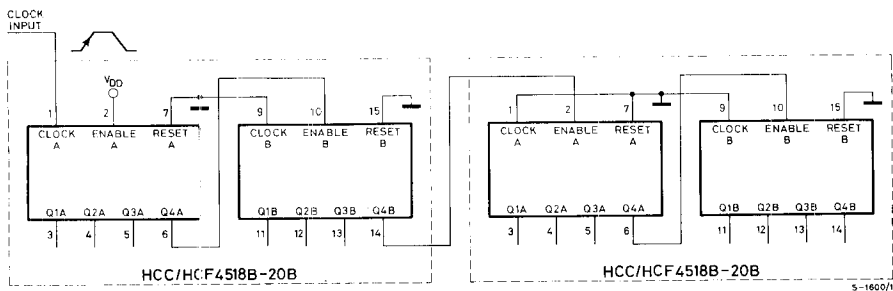
TYPICAL APPLICATIONS (continued)

Synchronous cascading of four binary counters with negative-edge triggering