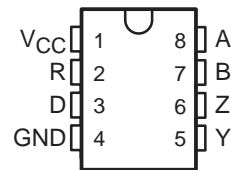


# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

SLLS003E – OCTOBER 1985 – REVISED JUNE 1998

- Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11
- Bus Voltage Range . . . -7 V to 12 V
- Positive- and Negative-Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal-Shutdown Protection
- Receiver Input Impedance . . . 12 k $\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

D OR P PACKAGE  
(TOP VIEW)



## description

The SN75179B is a differential driver and receiver pair designed for balanced transmission-line applications and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11. It is designed to improve the performance of full-duplex data communications over long bus lines.

The SN75179B driver output provides limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of  $\pm 200$  mV over a common-mode input voltage range of -7 V to 12 V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN75179B is designed to drive current loads of up to 60 mA maximum.

The SN75179B is characterized for operation from 0°C to 70°C.

## Function Tables

### DRIVER

| INPUT<br>D | OUTPUTS |   |
|------------|---------|---|
|            | Y       | Z |
| H          | H       | L |
| L          | L       | H |

### RECEIVER

| DIFFERENTIAL INPUTS<br>A - B | OUTPUT<br>R |
|------------------------------|-------------|
| $V_{ID} \geq 0.2$ V          | H           |
| $-0.2$ V $< V_{ID} < 0.2$ V  | ?           |
| $V_{ID} \leq -0.2$ V         | L           |
| Open                         | ?           |

H = high level, L = low level, ? = indeterminate



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

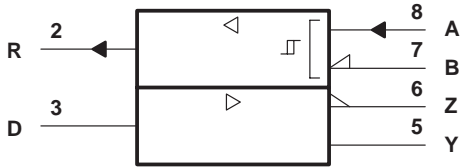
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# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

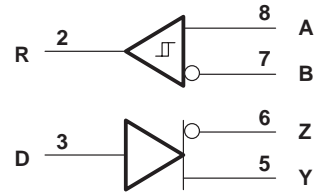
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## logic symbol†

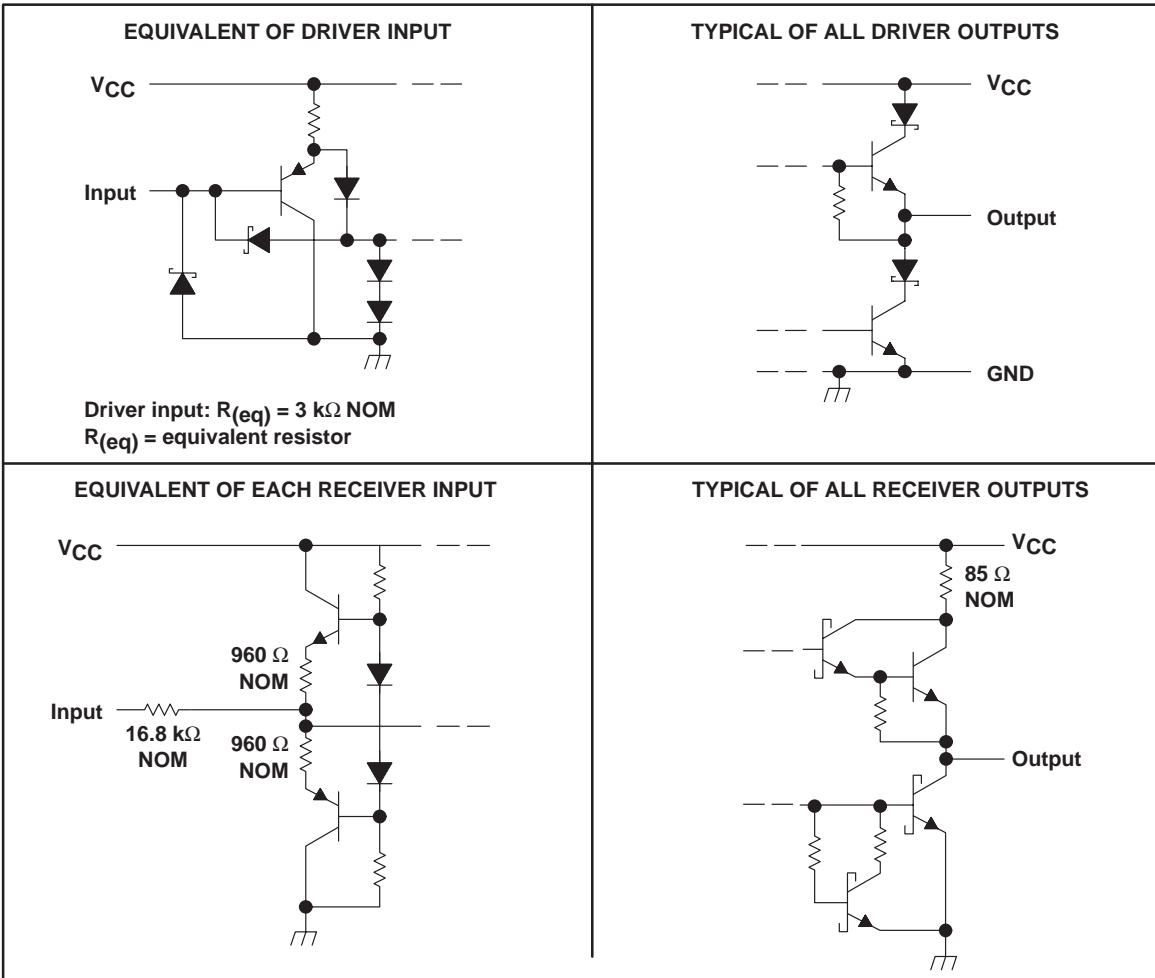


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematics of inputs and outputs



# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                |
|--|----------------|
| Supply voltage, $V_{CC}$ (see Note 1) .....                            | 7 V            |
| Voltage range at any bus terminal .....                                | –10 V to 15 V  |
| Differential input voltage, $V_{ID}$ (see Note 2) .....                | ±25 V          |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): D package ..... | 197°C/W        |
| P package .....  | 104°C/W        |
| Storage temperature range, $T_{stg}$ .....                             | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....     | 260°C          |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.  
 2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.  
 3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

|                                       |          | MIN  | NOM | MAX  | UNIT |
|---------------------------------------|----------|------|-----|------|------|
| Supply voltage, $V_{CC}$              |          | 4.75 | 5   | 5.25 | V    |
| High-level input voltage, $V_{IH}$    | Driver   | 2    |     |      | V    |
| Low-level input voltage, $V_{IL}$     | Driver   |      |     | 0.8  | V    |
| Common-mode input voltage, $V_{IC}$   |          | –7‡  |     | 12   | V    |
| Differential input voltage, $V_{ID}$  |          |      |     | ±12  | V    |
| High-level output current, $I_{OH}$   | Driver   |      |     | –60  | mA   |
|                                       | Receiver |      |     | –400 | µA   |
| Low-level output current, $I_{OL}$    | Driver   |      |     | 60   | mA   |
|                                       | Receiver |      |     | 8    |      |
| Operating free-air temperature, $T_A$ |          | 0    |     | 70   | °C   |

‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.



# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

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## DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS                                      | MIN                           | TYP† | MAX                                   | UNIT          |
|---|--|-------------------------------|------|---------------------------------------|---------------|
| $V_{IK}$ Input clamp voltage  | $I_I = -18 \text{ mA}$                               |                               |      | -1.5                                  | V             |
| $V_O$ Output voltage  | $I_O = 0$  | 0                             |      | 6                                     | V             |
| $ V_{OD1} $ Differential output voltage                             | $I_O = 0$  | 1.5                           |      | 6                                     | V             |
| $ V_{OD2} $ Differential output voltage                             | $R_L = 100 \Omega$ , See Figure 1                    | $1/2 V_{OD1}$ or $2^\ddagger$ |      |                                       | V             |
|   | $R_L = 54 \Omega$ , See Figure 1                     | 1.5                           | 2.5  | 5                                     | V             |
| $ V_{OD3} $ Differential output voltage                             | See Note 4   | 1.5                           |      | 5                                     | V             |
| $\Delta V_{OD} $ Change in magnitude of common-mode output voltage§ |  |                               |      | $\pm 0.2$                             | V             |
| $V_{OC}$ Common-mode output voltage                                 | $R_L = 54 \Omega$ or $100 \Omega$ , See Figure 1     |                               |      | $\begin{matrix} 3 \\ -1 \end{matrix}$ | V             |
| $\Delta V_{OC} $ Change in magnitude of common-mode output voltage§ |  |                               |      | $\pm 0.2$                             | V             |
| $I_O$ Output current  | $V_{CC} = 0$ , $V_O = -7 \text{ V to } 12 \text{ V}$ |                               |      | $\pm 100$                             | $\mu\text{A}$ |
| $I_{IH}$ High-level input current                                   | $V_I = 2.4 \text{ V}$                                |                               |      | 20                                    | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                                    | $V_I = 0.4 \text{ V}$                                |                               |      | -200                                  | $\mu\text{A}$ |
| $I_{OS}$ Short-circuit output current                               | $V_O = -7 \text{ V}$                                 |                               |      | -250                                  | mA            |
|   | $V_O = V_{CC}$ or $12 \text{ V}$                     |                               |      | 250                                   |               |
| $I_{CC}$ Supply current (total package)                             | No load  |                               | 57   | 70                                    | mA            |

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The minimum  $V_{OD2}$  with  $100\text{-}\Omega$  load is either  $1/2 V_{OD2}$  or  $2 \text{ V}$ , whichever is greater.

§  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input changes from a high level to a low level.

NOTE 4: See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER                                       | TEST CONDITIONS                  | MIN | TYP | MAX | UNIT |
|---|----------------------------------|-----|-----|-----|------|
| $t_{d(OD)}$ Differential output delay time      | $R_L = 54 \Omega$ , See Figure 3 |     | 15  | 22  | ns   |
| $t_{t(OD)}$ Differential output transition time |                                  |     | 20  | 30  | ns   |

## Symbol Equivalents

| DATA-SHEET PARAMETER | TIA/EIA-422-B             | TIA/EIA-485-A                          |
|----------------------|---------------------------|--|
| $V_O$                | $V_{Oa}, V_{Ob}$          | $V_{Oa}, V_{Ob}$                       |
| $ V_{OD1} $          | $V_o$                     | $V_o$                                  |
| $ V_{OD2} $          | $V_t (R_L = 100 \Omega)$  | $V_t (R_L = 54 \Omega)$                |
| $ V_{OD3} $          |                           | $V_t$ (Test Termination Measurement 2) |
| $\Delta V_{OD} $     | $  V_t  -  \bar{V}_t  $   | $  V_t  -  \bar{V}_t  $                |
| $V_{OC}$             | $ V_{os} $                | $ V_{os} $                             |
| $\Delta V_{OC} $     | $ V_{os} - \bar{V}_{os} $ | $ V_{os} - \bar{V}_{os} $              |
| $I_{OS}$             | $ I_{sa} ,  I_{sb} $      |  |
| $I_O$                | $ I_{xa} ,  I_{xb} $      | $I_{ia}, I_{ib}$                       |



## RECEIVER SECTION

**electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS  | MIN   | TYP† | MAX  | UNIT       |
|--|--|-------|------|------|------------|
| $V_{IT+}$ Positive-going input threshold voltage     | $V_O = 2.7\text{ V}$ , $I_O = -0.4\text{ mA}$                                |       |      | 0.2  | V          |
| $V_{IT-}$ Negative-going input threshold voltage     | $V_O = 0.5\text{ V}$ , $I_O = 8\text{ mA}$                                   | -0.2‡ |      |      | V          |
| $V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |  |       | 50   |      | mV         |
| $V_{OH}$ High-level output voltage                   | $V_{ID} = 200\text{ mV}$ , $I_{OH} = -400\text{ }\mu\text{A}$ , See Figure 2 |       | 2.7  |      | V          |
| $V_{OL}$ Low-level output voltage                    | $V_{ID} = -200\text{ mV}$ , $I_{OL} = 8\text{ mA}$ , See Figure 2            |       |      | 0.45 | V          |
| $I_I$ Line input current                             | Other input at 0 V, See Note 5   |       |      | 1    | mA         |
|  |  |       |      | -0.8 |            |
| $r_i$ Input resistance                               |  |       | 12   |      | k $\Omega$ |
| $I_{OS}$ Short-circuit output current                |  | -15   |      | -85  | mA         |
| $I_{CC}$ Supply current (total package)              | No load  |       | 57   | 70   | mA         |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: Refer to TIA/EIA-422-B for exact conditions.

**switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

| PARAMETER   | TEST CONDITIONS   | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low- to high-level output | $V_{ID} = -1.5\text{ V}$ to $1.5\text{ V}$ ,<br>$C_L = 15\text{ pF}$ , See Figure 4 |     | 19  | 35  | ns   |
| $t_{PHL}$ Propagation delay time, high- to low-level output |   |     | 30  | 40  | ns   |

## PARAMETER MEASUREMENT INFORMATION

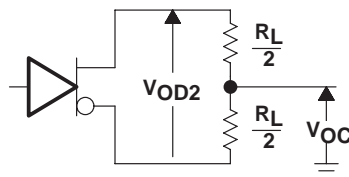


Figure 1. Driver  $V_{DD}$  and  $V_{OC}$

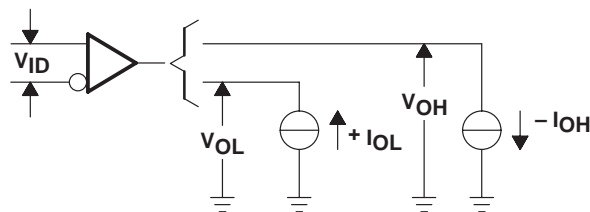
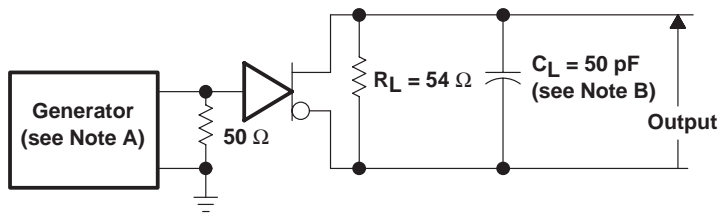


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$

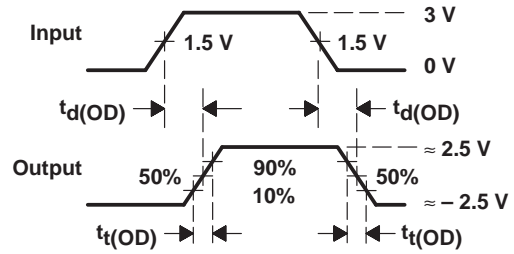
# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

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## PARAMETER MEASUREMENT INFORMATION (CONTINUED)



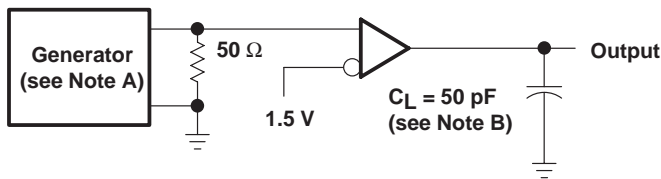
TEST CIRCUIT



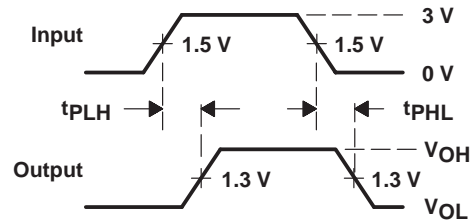
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

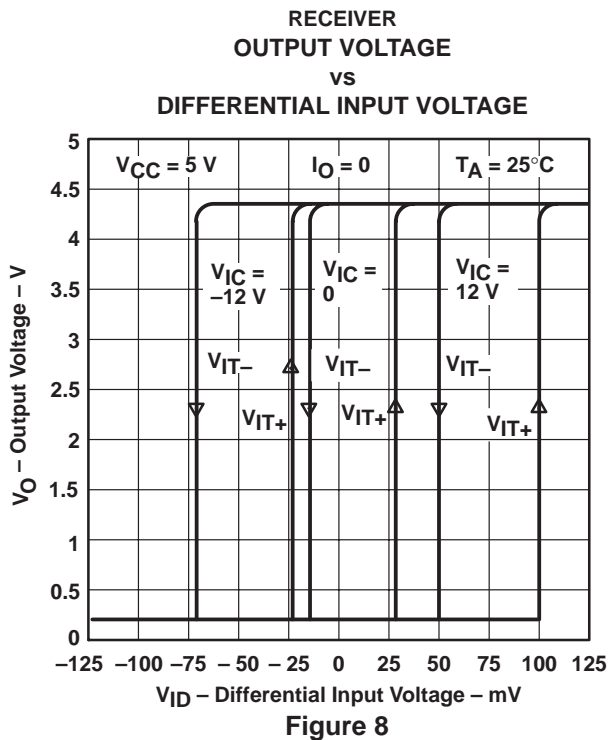
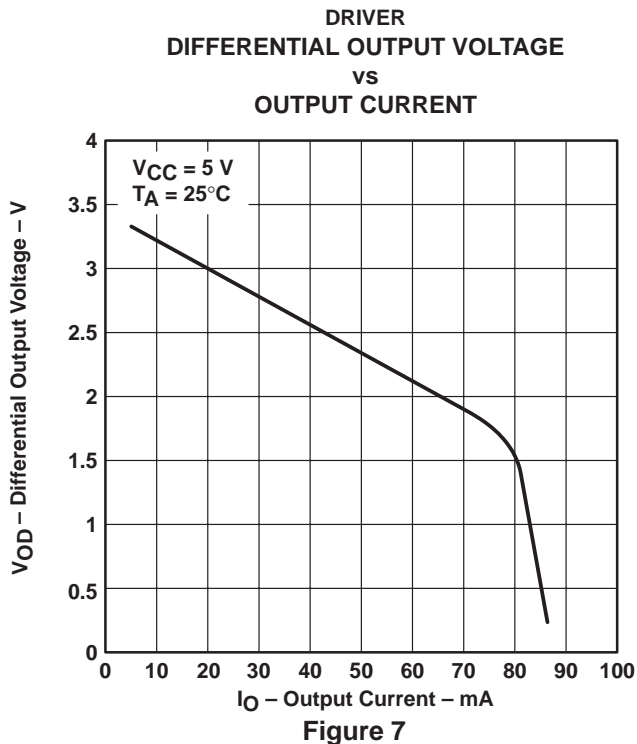
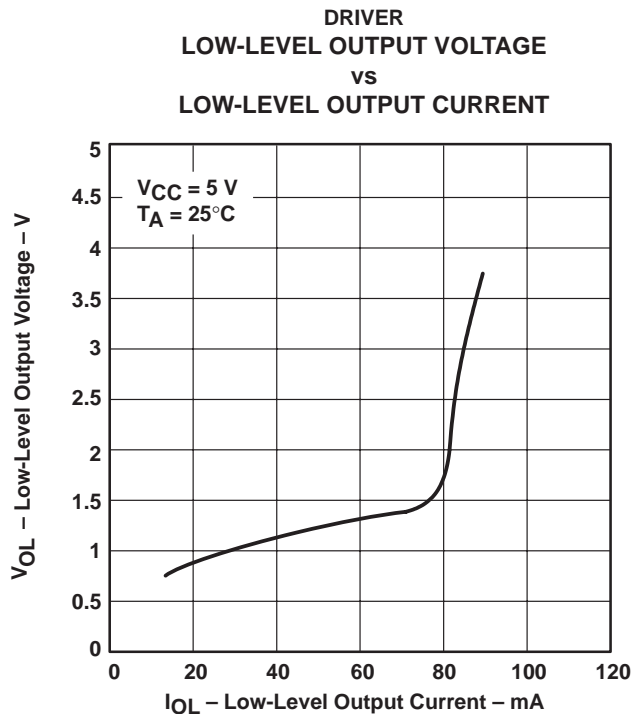
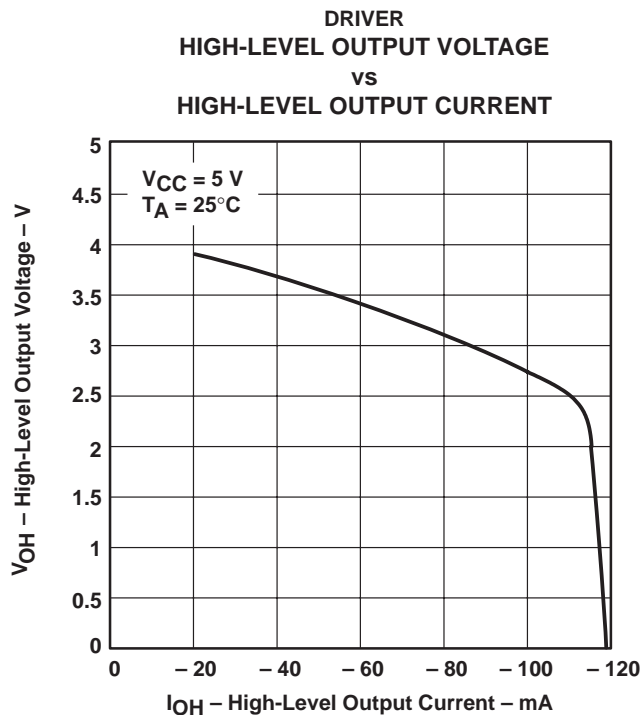


VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 4. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



# SN75179B DIFFERENTIAL DRIVER AND RECEIVER PAIR

SLLS003E – OCTOBER 1985 – REVISED JUNE 1998

## TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE  
vs  
HIGH-LEVEL OUTPUT CURRENT

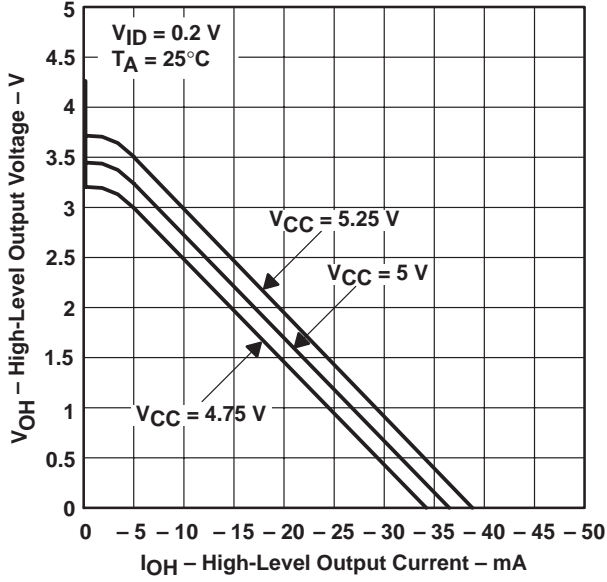


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

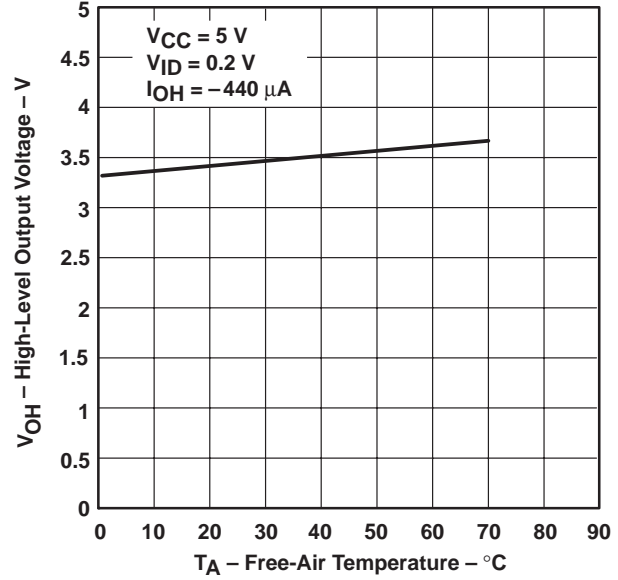


Figure 10

RECEIVER  
LOW-LEVEL OUTPUT VOLTAGE  
vs  
LOW-LEVEL OUTPUT CURRENT

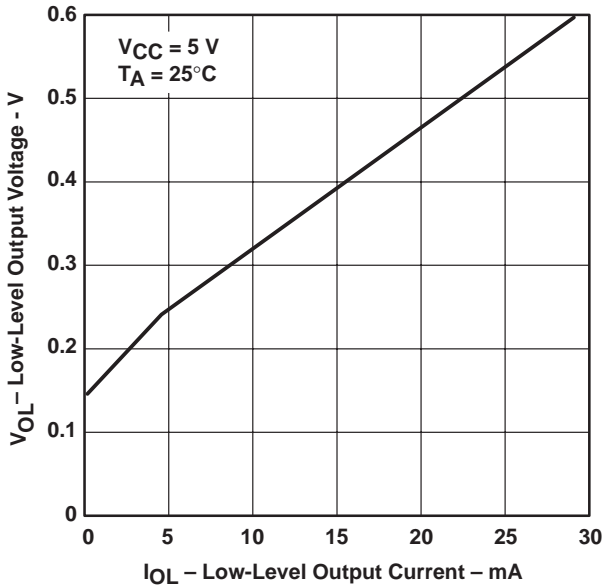


Figure 11

RECEIVER  
LOW-LEVEL OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

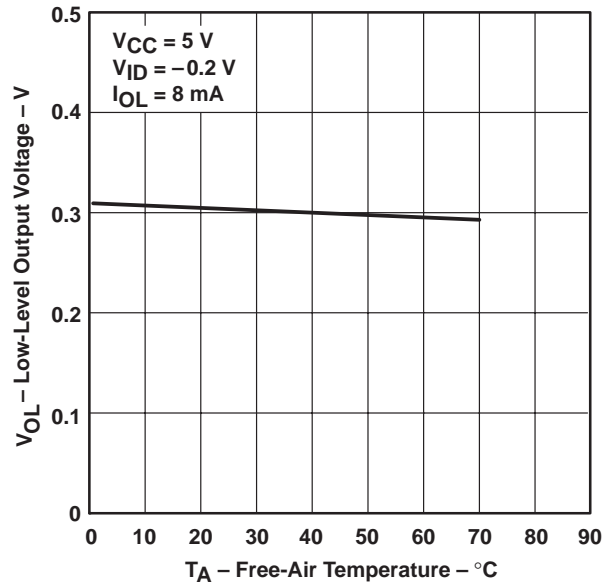


Figure 12



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75179BD        | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75179B                  | <a href="#">Samples</a> |
| SN75179BDE4      | ACTIVE        | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75179B                  | <a href="#">Samples</a> |
| SN75179BDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75179B                  | <a href="#">Samples</a> |
| SN75179BDRG4     | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 75179B                  | <a href="#">Samples</a> |
| SN75179BP        | ACTIVE        | PDIP         | P               | 8    | 50          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75179BP               | <a href="#">Samples</a> |
| SN75179BPE4      | ACTIVE        | PDIP         | P               | 8    | 50          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | SN75179BP               | <a href="#">Samples</a> |
| SN75179BPSR      | ACTIVE        | SO           | PS              | 8    | 2000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | A179B                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75179BDR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75179BDR | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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