

LM118-N/LM218-N/LM318-N Operational Amplifiers

Check for Samples: [LM118-N](#), [LM218-N](#), [LM318-N](#)

FEATURES

- 15 MHz Small Signal Bandwidth
- Ensured 50V/μs Slew Rate
- Maximum Bias Current of 250 nA
- Operates from Supplies of ±5V to ±20V
- Internal Frequency Compensation
- Input and Output Overload Protected
- Pin Compatible with General Purpose Op Amps

DESCRIPTION

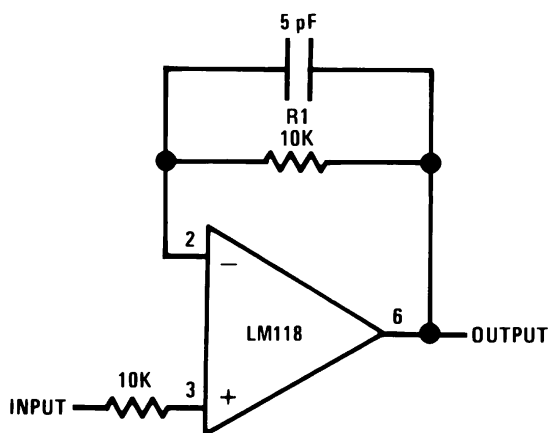
The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM218-N is identical to the LM118 except that the LM218-N has its performance specified over a -25°C to +85°C temperature range. The LM318-N is specified from 0°C to +70°C.

Fast Voltage Follower


Do not hard-wire as voltage follower ($R1 \geq 5 \text{ k}\Omega$)


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage	±20V
Power Dissipation ⁽³⁾	500 mW
Differential Input Current ⁽⁴⁾	±10 mA
Input Voltage ⁽⁵⁾	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
lm118-n	–55°C to +125°C
LM218-N	–25°C to +85°C
LM318-N	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
TO-99 Package	300°C
PDIP Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
SOIC Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Tolerance ⁽⁶⁾	2000V

- (1) Refer to RETS118X for LM118H and LM118J military specifications.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
- (3) The maximum junction temperature of the lm118-n is 150°C, the LM218-N is 110°C, and the LM318-N is 110°C. For operating at elevated temperatures, devices in the LMC package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
- (4) The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
- (5) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- (6) Human body model, 1.5 kΩ in series with 100 pF.

Electrical Characteristics⁽¹⁾

Parameter	Conditions	LM118-N/LM218-N			LM318-N			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25^\circ\text{C}$		2	4		4	10	mV
Input Offset Current	$T_A = 25^\circ\text{C}$		6	50		30	200	nA
Input Bias Current	$T_A = 25^\circ\text{C}$		120	250		150	500	nA
Input Resistance	$T_A = 25^\circ\text{C}$	1	3		0.5	3		MΩ
Supply Current	$T_A = 25^\circ\text{C}$		5	8		5	10	mA
Large Signal Voltage Gain	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$	50	200		25	200		V/mV
Slew Rate	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $A_V = 1$ (2)	50	70		50	70		V/μs
Small Signal Bandwidth	$T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA

- (1) These specifications apply for $\pm 5\text{V} \leq V_S \leq \pm 20\text{V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (lm118-n), $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ (LM218-N), and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (LM318-N). Also, power supplies must be bypassed with 0.1 μF disc capacitors.
- (2) Slew rate is tested with $V_S = \pm 15\text{V}$. The lm118-n is in a unity-gain non-inverting configuration. V_{IN} is stepped from –7.5V to +7.5V and vice versa. The slew rates between –5.0V and +5.0V and vice versa are tested and specified to exceed 50V/μs.

Electrical Characteristics ⁽¹⁾ (continued)

Parameter	Conditions	LM118-N/LM218-N			LM318-N			Units
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current				500			750	nA
Supply Current	$T_A = 125^\circ\text{C}$		4.5	7				mA
Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{ k}\Omega$	25			20			V/mV
Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 2\text{ k}\Omega$	± 12	± 13		± 12	± 13		V
Input Voltage Range	$V_S = \pm 15\text{V}$	± 11.5			± 11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

TYPICAL PERFORMANCE CHARACTERISTICS

LM118-N, LM218-N

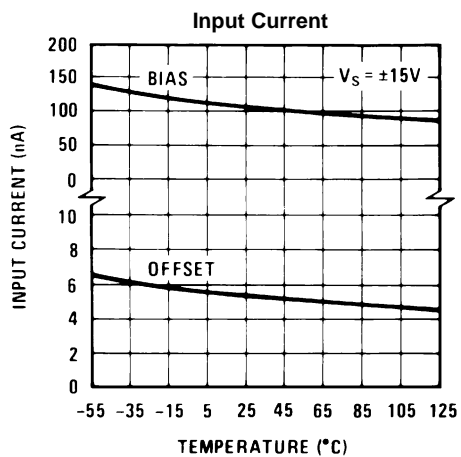


Figure 1.

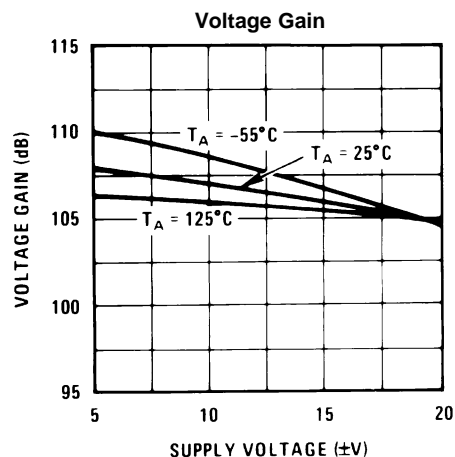


Figure 2.

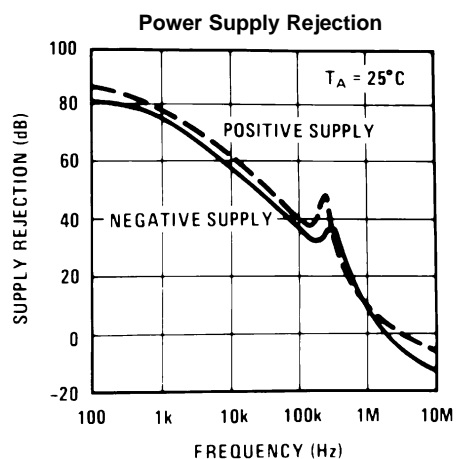


Figure 3.

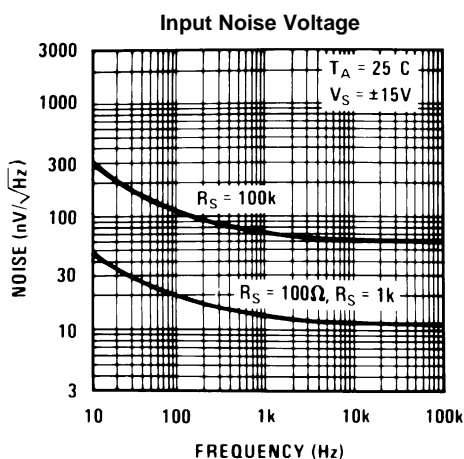


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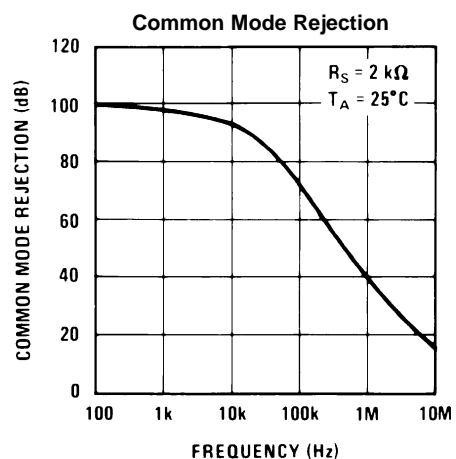


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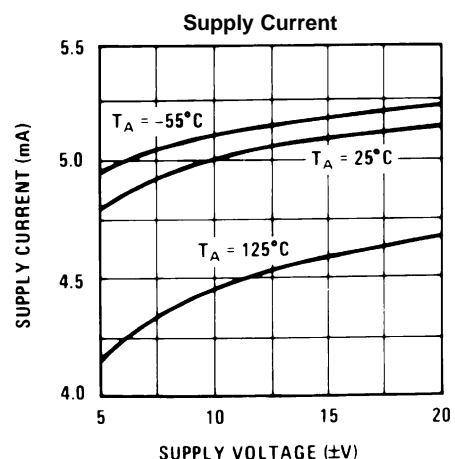


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

Closed Loop Output Impedance

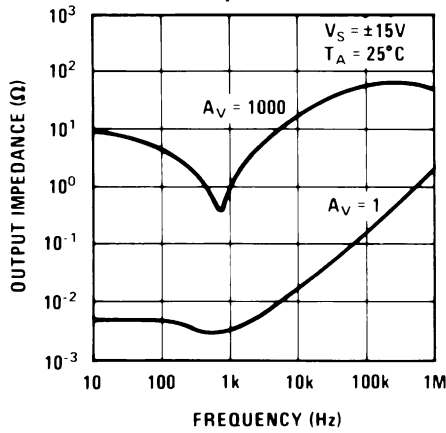


Figure 7.

Current Limiting

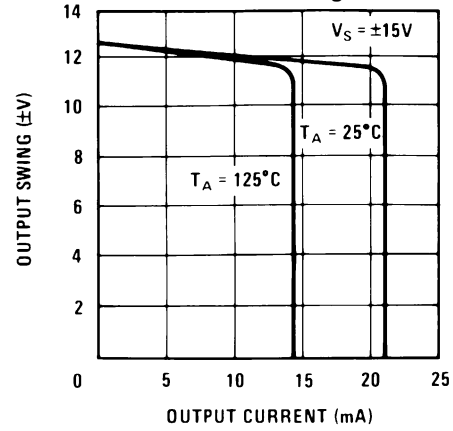


Figure 8.

Input Current

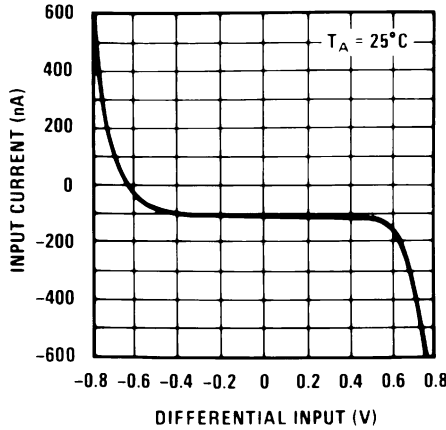


Figure 9.

Unity Gain Bandwidth

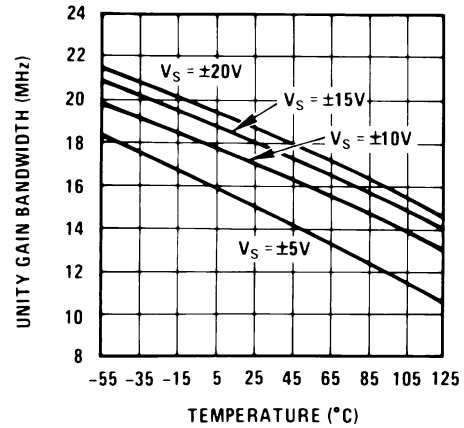


Figure 10.

Voltage Follower Slew Rate

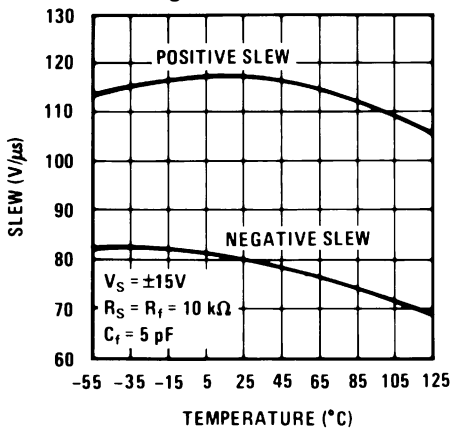


Figure 11.

Inverter Settling Time

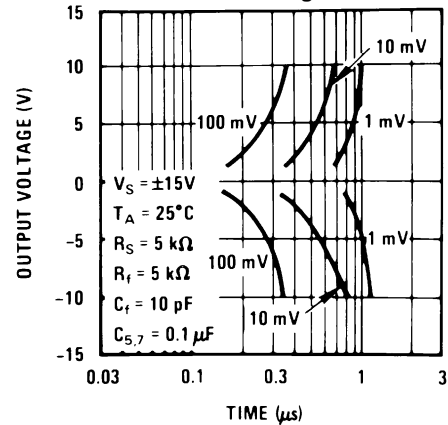


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

LM118-N, LM218-N

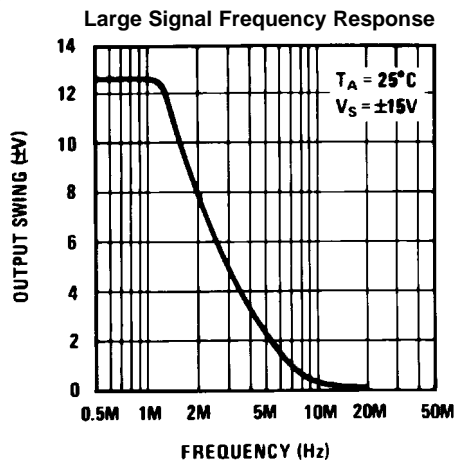


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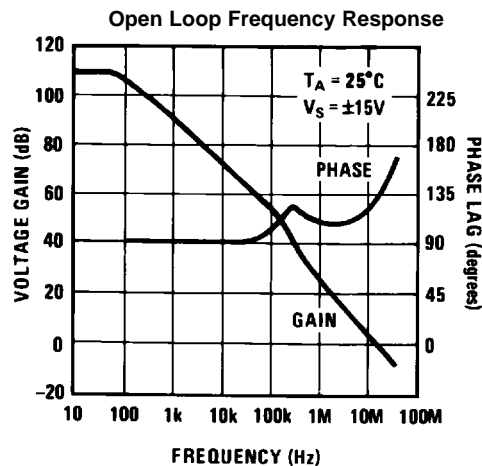


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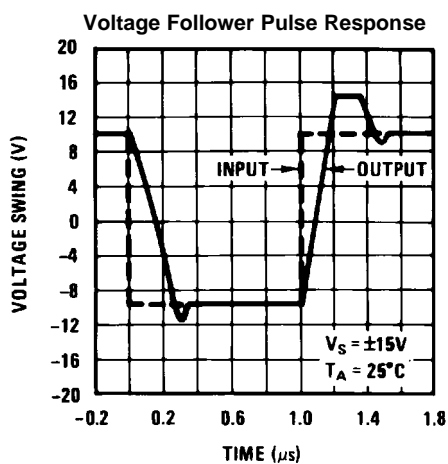


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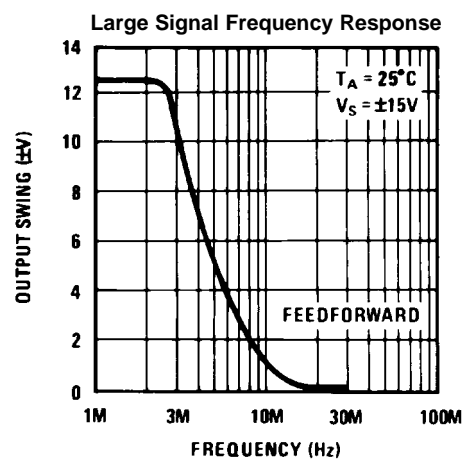


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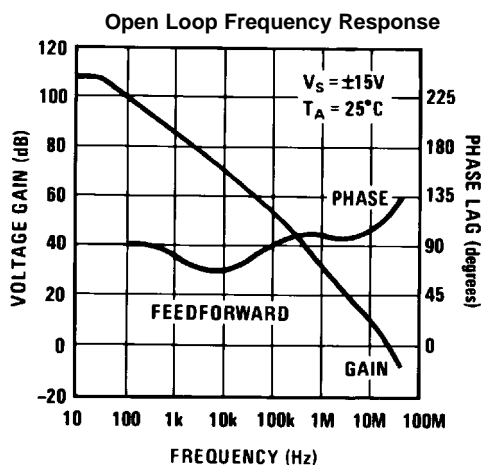


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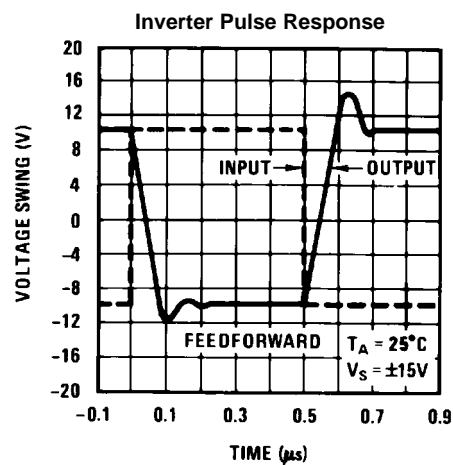


Figure 18.

Typical Performance Characteristics

LM318-N

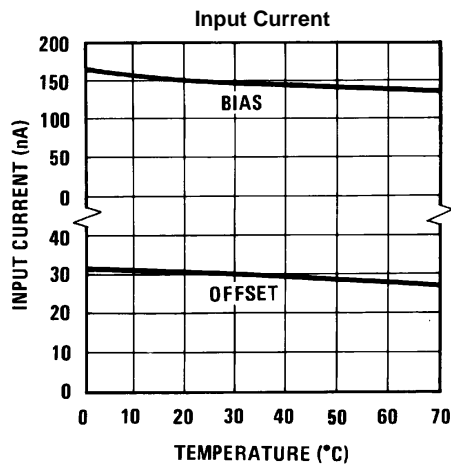


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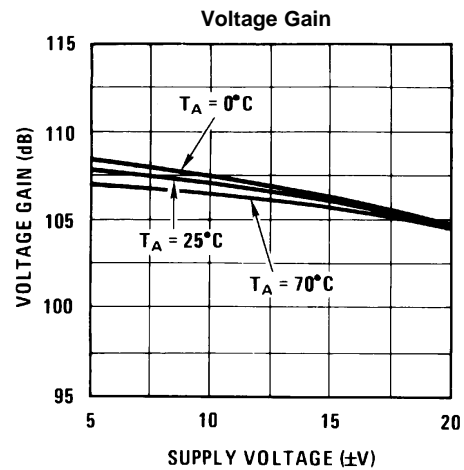


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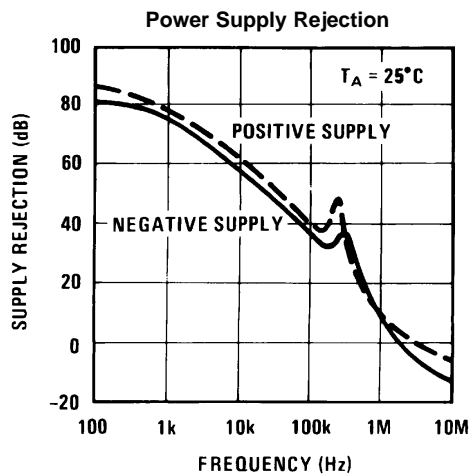


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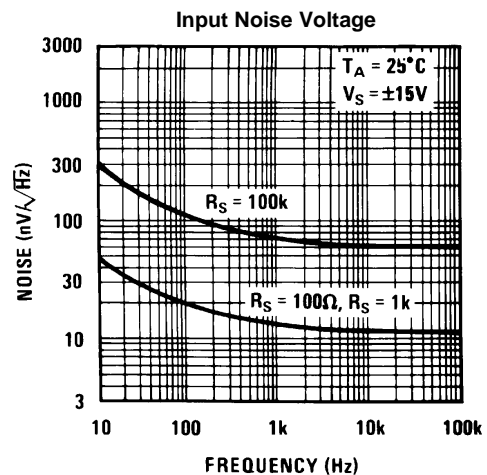


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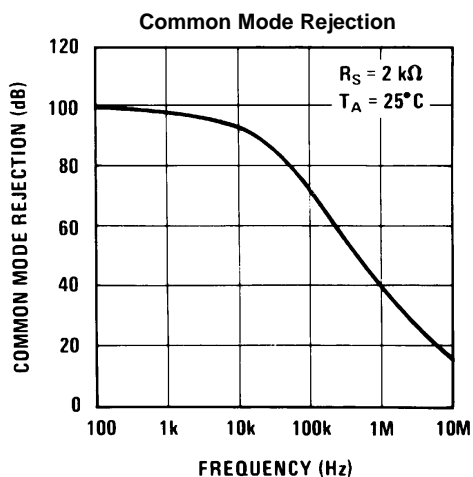


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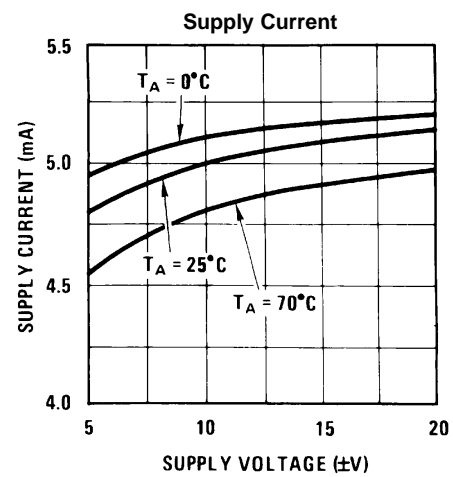
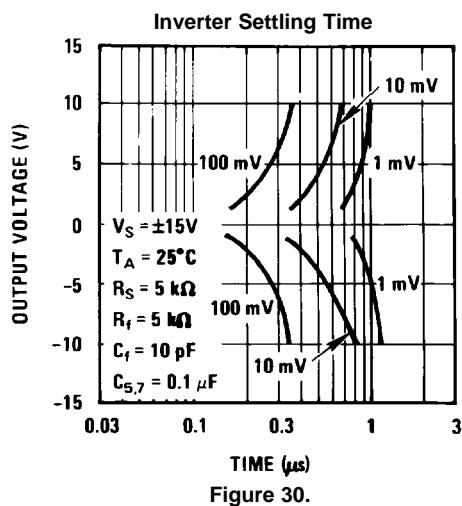
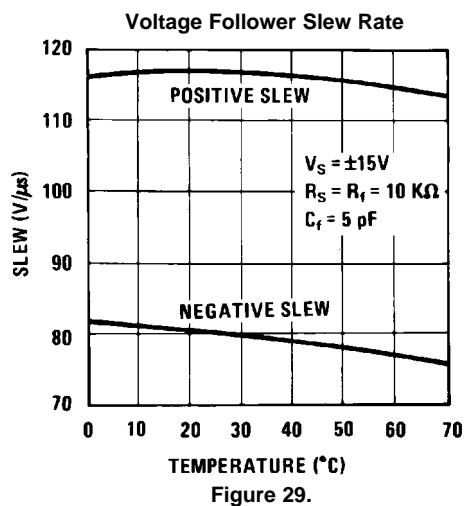
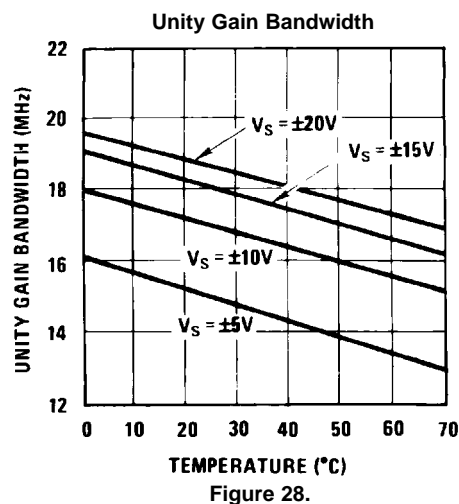
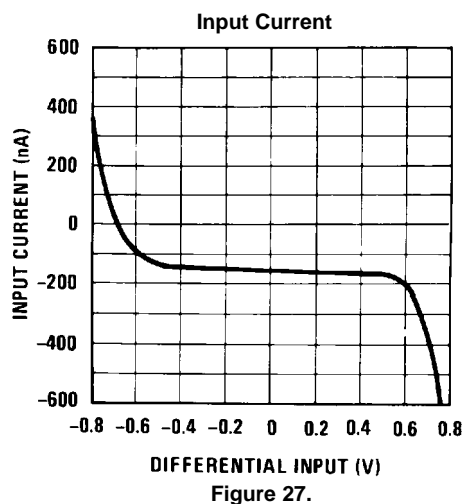
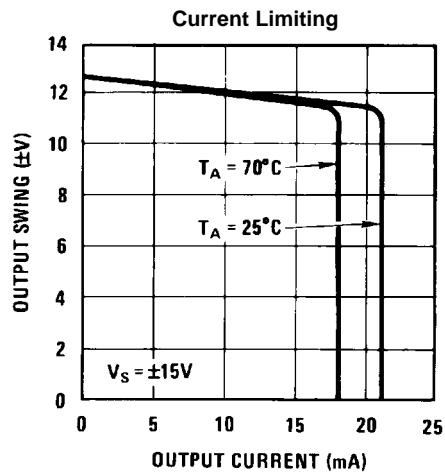
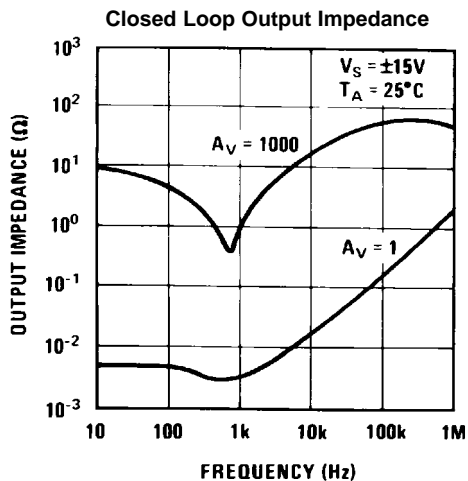


Figure 24.

Typical Performance Characteristics (continued)

LM318-N



Typical Performance Characteristics (continued)

LM318-N

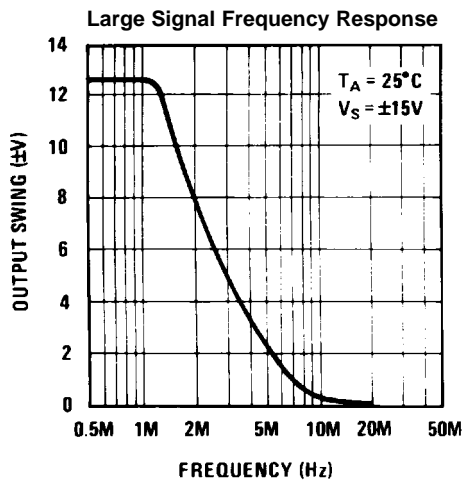


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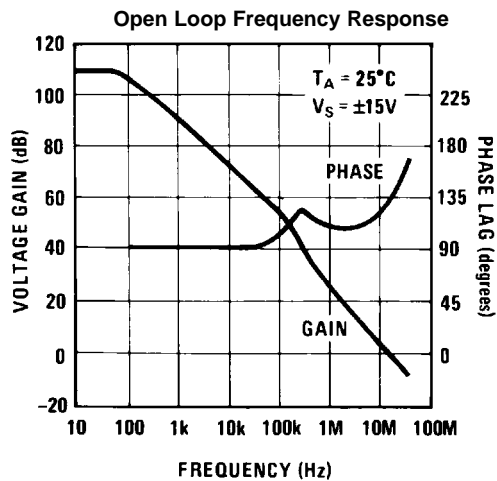


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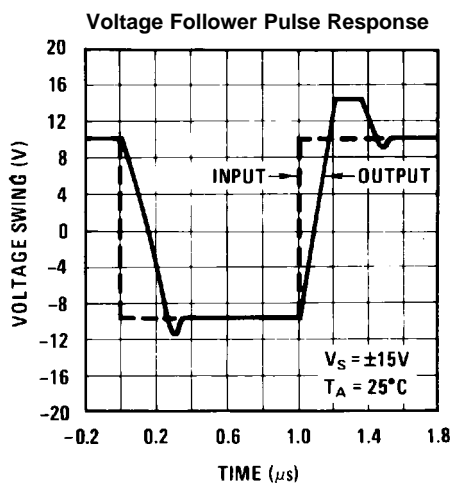


Figure 33.

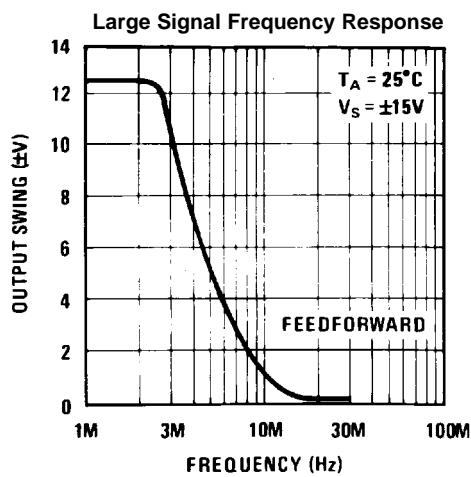


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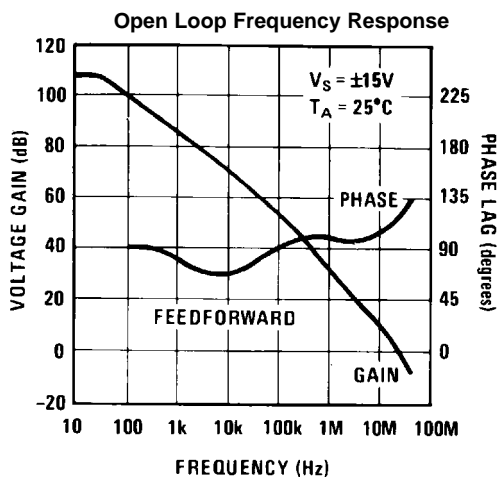


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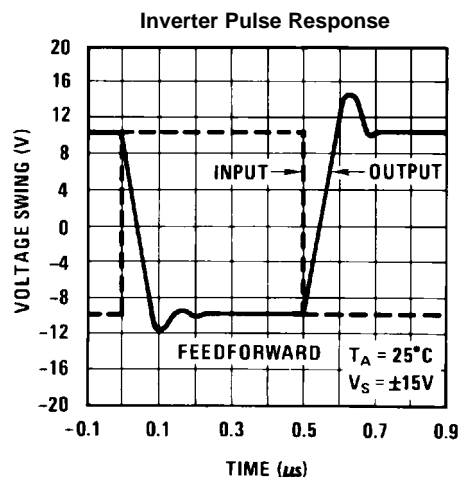
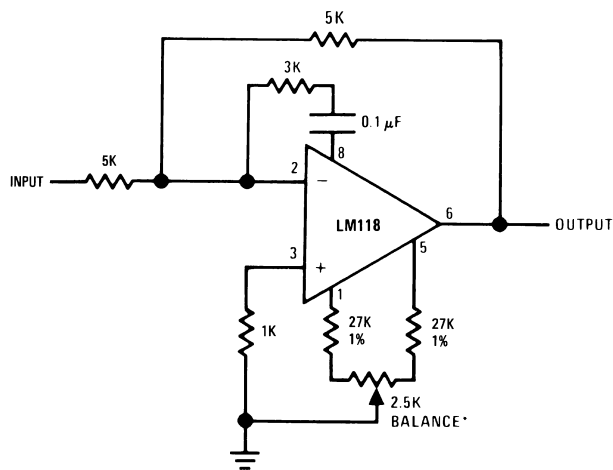


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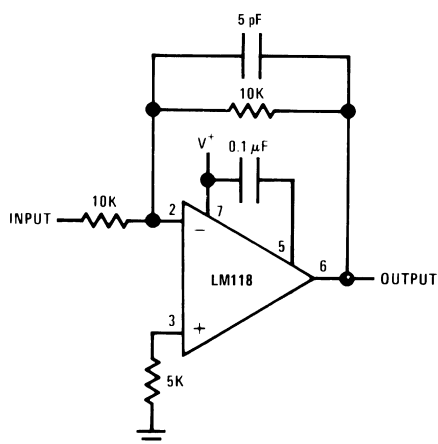
AUXILIARY CIRCUITS



*Balance circuit necessary for increased slew.

Slew rate typically 150V/μs.

Figure 37. Feedforward Compensation for Greater Inverting Slew Rate



Slew and settling time to 0.1% for a 10V step change is 800 ns.

Figure 38. Compensation for Minimum Settling Time

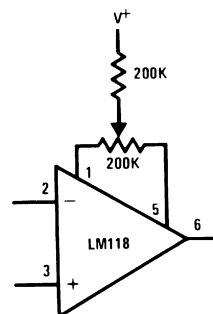


Figure 39. Offset Balancing

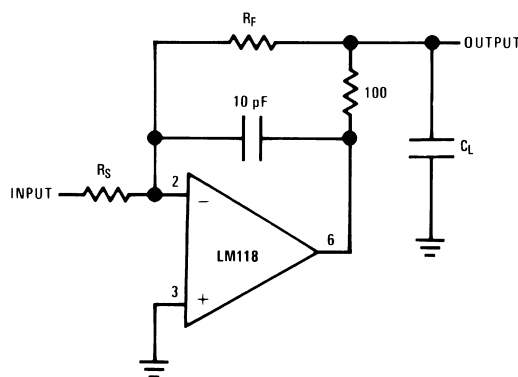


Figure 40. Isolating Large Capacitive Loads

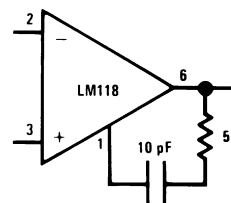
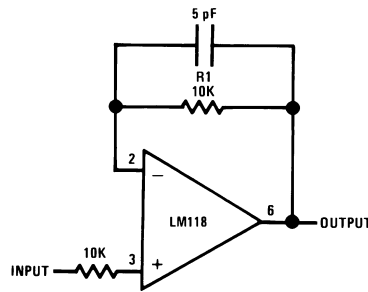


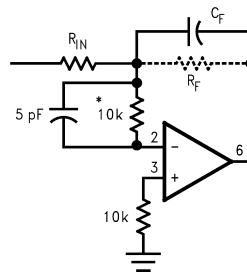
Figure 41. Overcompensation

TYPICAL APPLICATIONS



Do not hard-wire as voltage follower ($R_1 \geq 5 \text{ k}\Omega$)

Figure 42. Fast Voltage Follower



$C_F = \text{Large}$
($C_F \geq 50 \text{ pF}$)

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

Do not hard-wire as voltage follower ($R_1 \geq 5 \text{ k}\Omega$)

Figure 43.

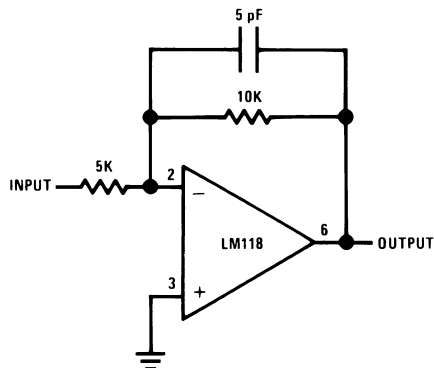


Figure 44. Fast Summing Amplifier

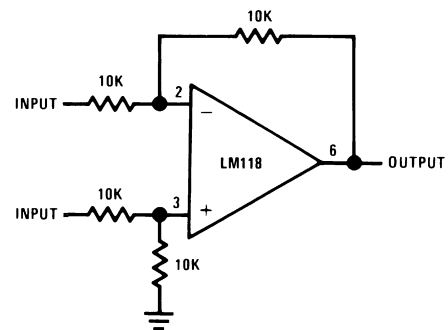


Figure 45. Differential Amplifier

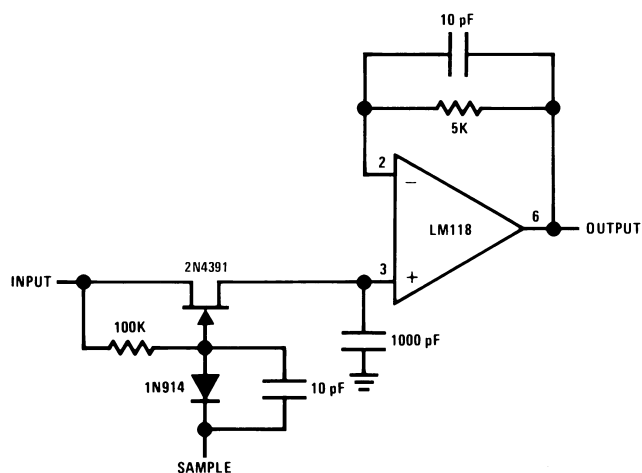
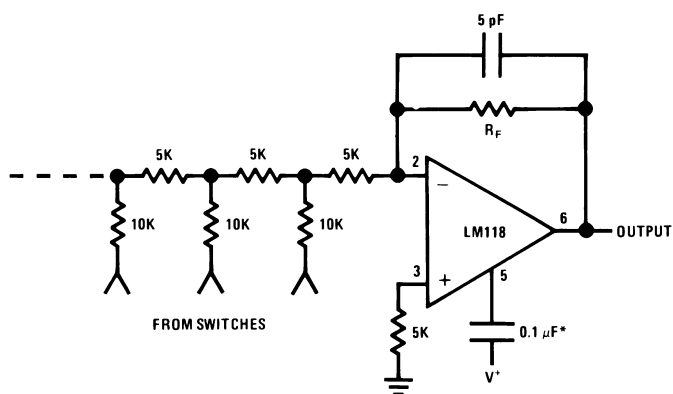
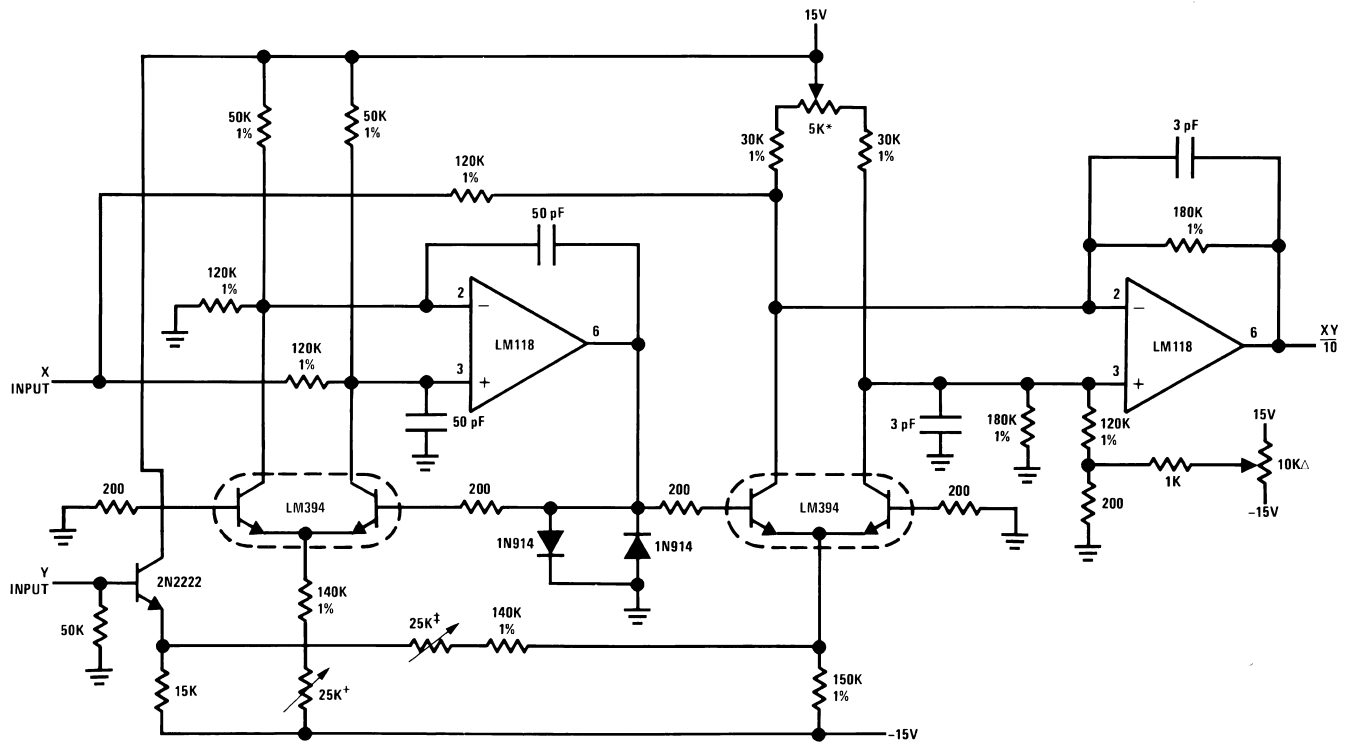


Figure 46. Fast Sample and Hold



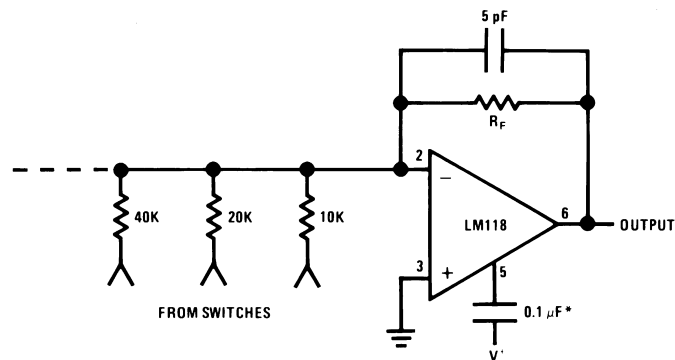
*Optional—Reduces settling time.

Figure 47. D/A Converter Using Ladder Network



ΔOutput zero.
 *"Y" zero
 + "X" zero
 ‡Full scale adjust.

Figure 48. Four Quadrant Multiplier



*Optional—Reduces settling time.

Figure 49. D/A Converter Using Binary Weighted Network

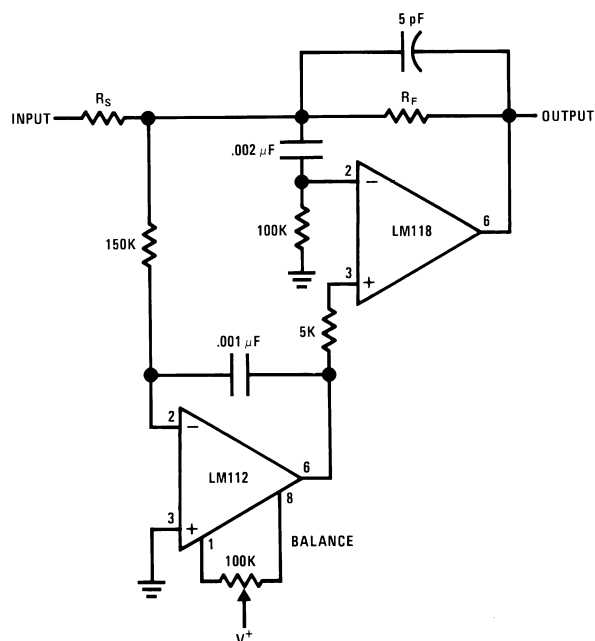
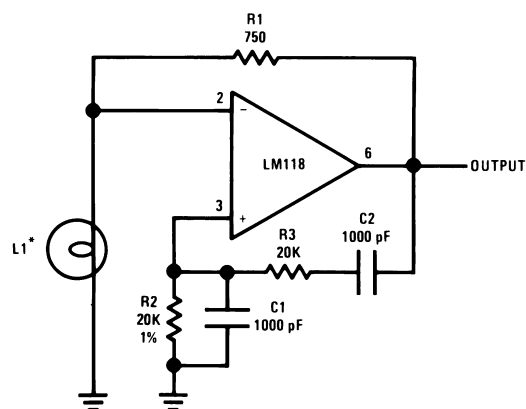


Figure 50. Fast Summing Amplifier with Low Input Current

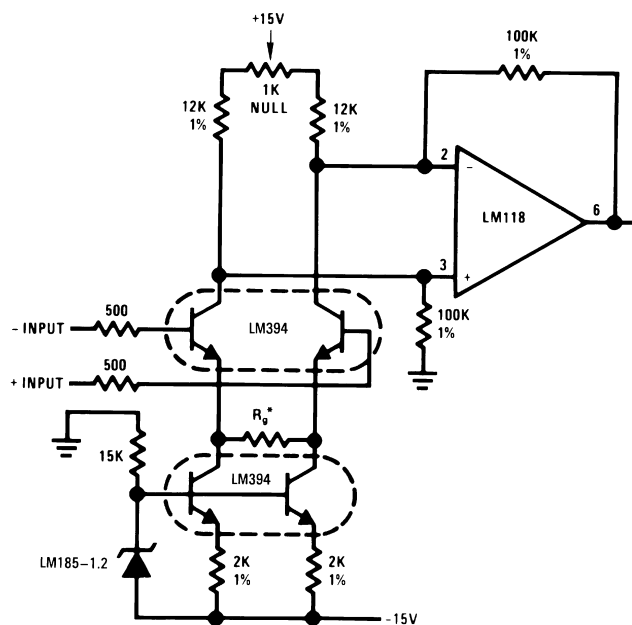


*L1—10V—14 mA bulb ELDEMA 1869

$$R1 = R2$$
$$C1 = C2$$

$$f = \frac{1}{2\pi R_2 C_1}$$

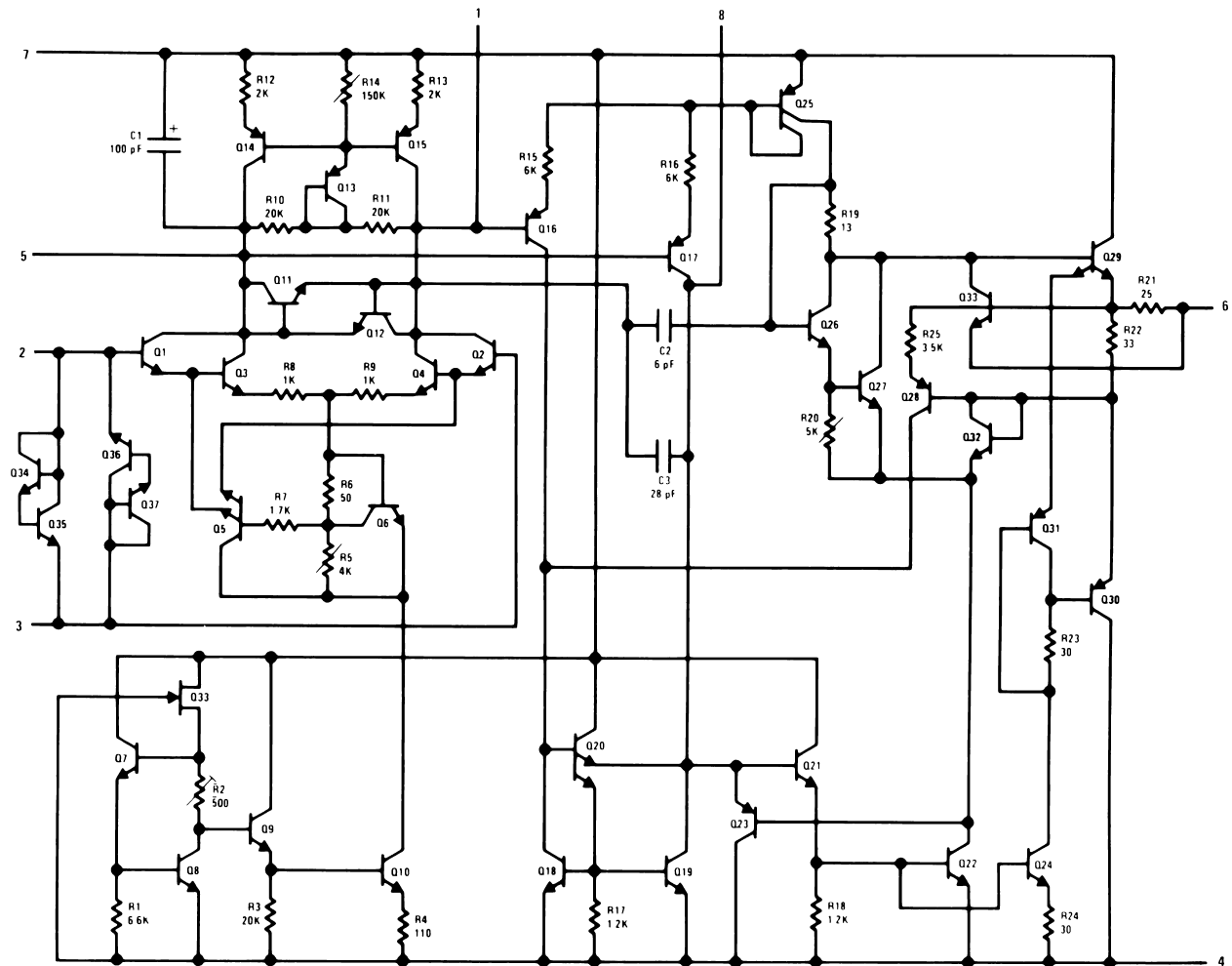
Figure 51. Wein Bridge Sine Wave Oscillator



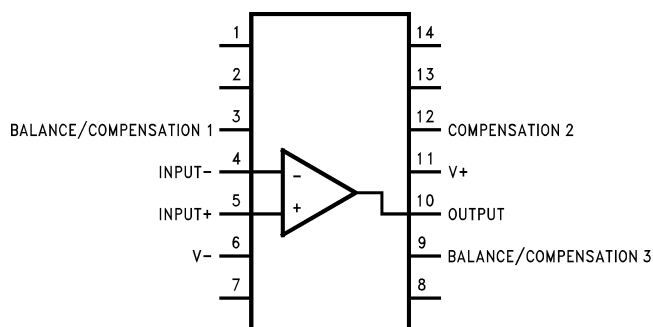
$$*Gain \geq \frac{200K}{R_g} \text{ for } 1.5K \leq R_g \leq 200K$$

Figure 52. Instrumentation Amplifier

Schematic Diagram

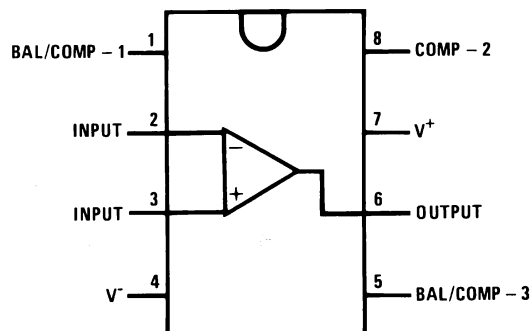


Pin Diagram



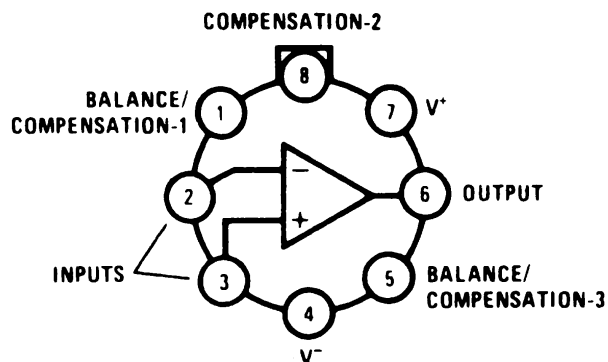
Available per JM38510/10107.

**Dual-In-Line Package
(Top View)**
See Package Number J (R-GDIP-T14)



Available per JM38510/10107.

**Dual-In-Line Package
(Top View)**
See Package Number NAB008A, D (R-PDSO-G8),
or P (R-PDIP-T8)



Pin connections shown on schematic diagram and typical applications are for TO-99 package.

**TO-99 Package
(Top View)**
See Package Number LMC (O-MBCY-W8)

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C

Page

- Changed layout of National Data Sheet to TI format [16](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM118H	ACTIVE	TO-99	LMC	8	500	TBD	Call TI	Call TI	-55 to 125	LM118H	Samples
LM118H/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	-55 to 125	LM118H	Samples
LM318M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM 318M	
LM318M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	SN CU SN	Level-1-260C-UNLIM	0 to 70	LM 318M	Samples
LM318MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	SN CU SN	Level-1-260C-UNLIM	0 to 70	LM 318M	Samples
LM318N	NRND	PDIP	P	8	40	TBD	Call TI	Call TI	0 to 70	LM 318N	
LM318N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	SN CU SN	Level-1-NA-UNLIM	0 to 70	LM 318N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM318MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

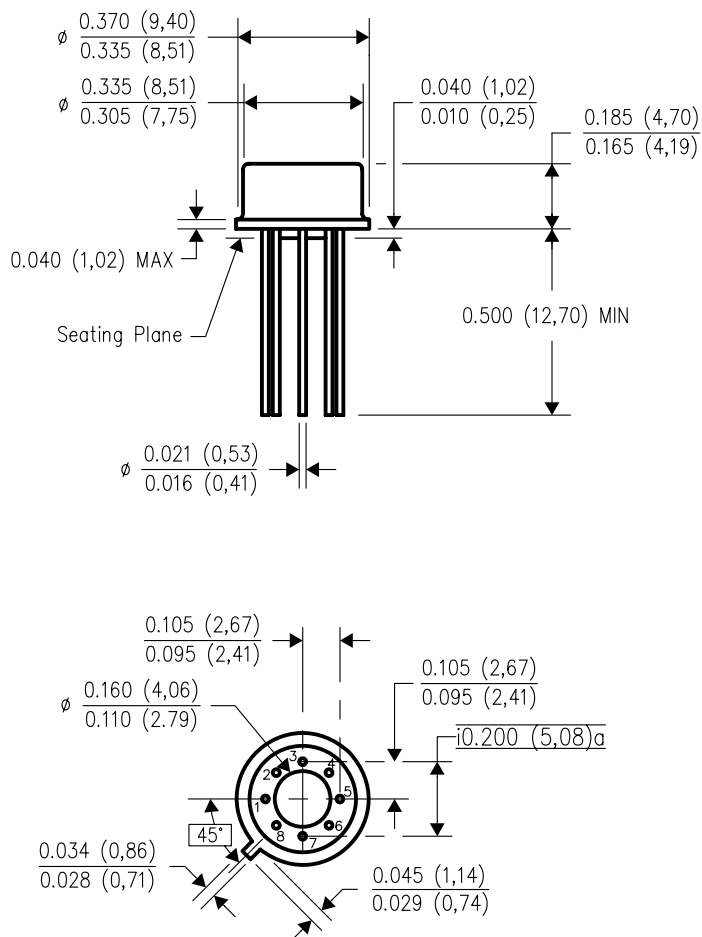


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM318MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

LMC (O-MBCY-W8)

METAL CYLINDRICAL PACKAGE



4202483/B 09/07

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
 - Pin numbers shown for reference only. Numbers may not be marked on package.
 - Falls within JEDEC MO-002/TO-99.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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