MC54/74HC266

Product Preview

Quad 2-Input Exclusive NOR Gate with Open-Drain Outputs

High-Performance Silicon-Gate CMOS

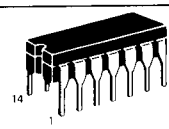
The MC54/74HC266 is identical in pinout to the LS266. The HC266 inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC266 output is a high-performance MOS N-Channel FET. Therefore, with suitable output pullup resistors, this gate can be used in wired AND applications. Using the output characteristic curves in this data sheet, this device can be used as an LED driver, or in any application that only requires a sinking current.

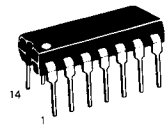
To comply with JEDEC Standard No. 7A, Motorola's HC266 manufactured after the date code 8547 has open-drain outputs. HC266 prior to the date code 8547 has standard CMOS outputs. (See Figure 4 for date code identifier.)

For applications requiring Standard CMOS outputs, use the HC7266.

- Output Drive Capability: 10 LSTTL Loads with Suitable Pullup Resistor
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 52 FETs or 13 Equivalent Gates



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

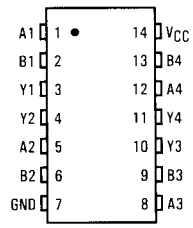
D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

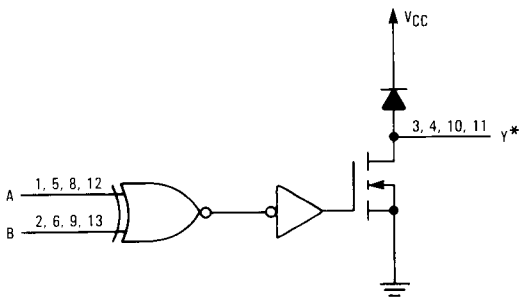
MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

$T_A = -55°$ to 125°C for all packages.
Dimensions in Chapter 7.

PIN ASSIGNMENT



LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

*Denotes Open-Drain Outputs

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	Z
L	H	L
H	L	L
H	H	Z

Z = high impedance

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \le (V_{in}$ or $V_{out}) \le V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0 V	0	1000	ns
	(Figure 1)	V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V, I_{out} = 0 μA	2.0	1.5	1.5	1.5	V
		or V_{out} = V_{CC} − 0.1 V,	4.5	3.15	3.15	3.15	
		R_{pu} per Figure 2	6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V, I_{out} = 0 μA	2.0	0.3	0.3	0.3	V
		or V_{out} = V_{CC} − 0.1 V,	4.5	0.9	0.9	0.9	
		R_{pu} per Figure 2	6.0	1.2	1.2	1.2	
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL}	2.0	0.1	0.1	0.1	V
		$\|I_{out}\| \le 20$ μA	4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 4.0$ mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\| \le 5.2$ mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High-Impedance State	6.0	±0.5	±5.0	±10.0	μA
		V_{in} = V_{IL} or V_{IH}					
		V_{out} = V_{CC} or GND					
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND	6.0	2	20	40	μA
		I_{out} = 0 μA					

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLZ}, t_{PZL}	Maximum Propagation Delay, (Figures 1 and 2)	2.0 4.5 6.0	120 24 20	150 30 26	180 36 31	ns
t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 4.5 6.0	75 15 13	95 19 16	110 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Gate) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 11	pF

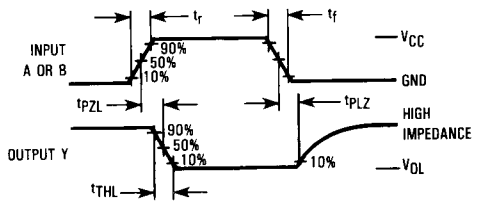
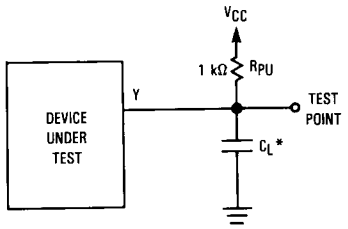
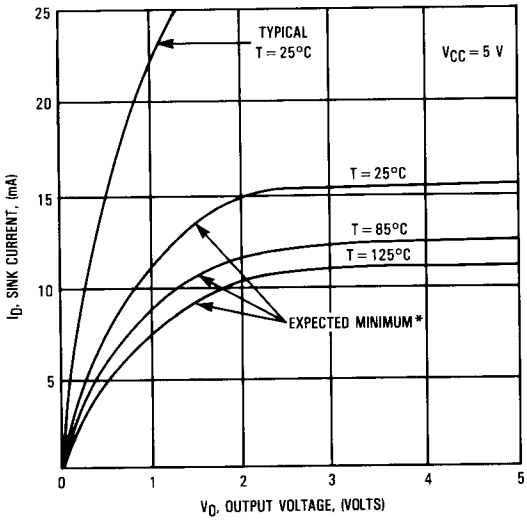


Figure 1. Switching Waveforms



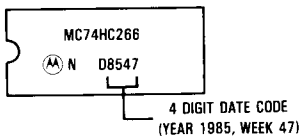
*Includes all probe and jig capacitance.

Figure 2. Test Circuit

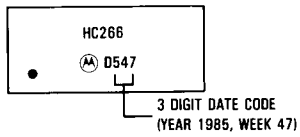


*The expected minimum curves are not guarantees, but are design aids.

Figure 3. Open-Drain Output Characteristics



4a. DIP

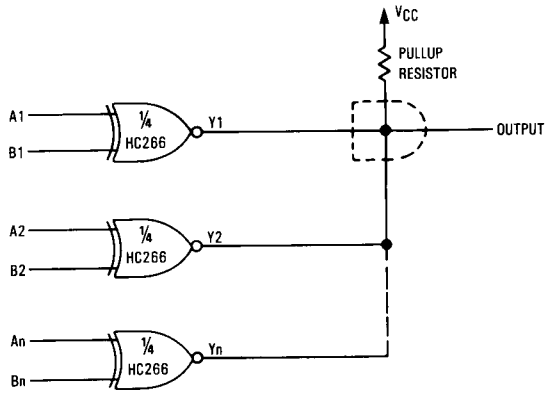


4b. SOIC

Figure 4. Date Code Identifier

TYPICAL APPLICATIONS

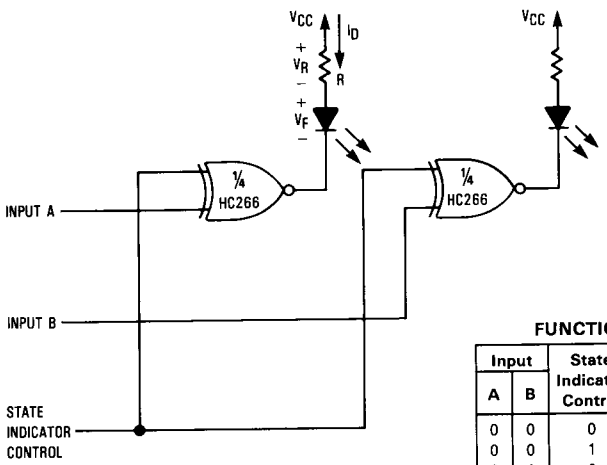
WIRED AND



$OUTPUT = Y1 \bullet Y2 \ldots \bullet Yn$

$= \overline{A1 \oplus B1 \bullet A2 \oplus B2 \cdots \bullet An \oplus Bn}$

STATE INDICATOR WITH LED DRIVER CIRCUIT



DESIGN EXAMPLE

CONDITIONS: $I_D \cong 10$ mA

USING FIGURE 3 TYPICAL CURVE, @ $I_D = 10$ mA, $V_{DS} \cong 0.4$ V

$$\therefore R = \frac{V_{CC} - V_F - V_O}{I_D}$$

$$= \frac{5\text{ V} - 1.7\text{ V} - 0.4\text{ V}}{10\text{ mA}}$$

$= 290\ \Omega$

Use R = 270 Ω

FUNCTION TABLE

Input A	Input B	State Indicator Control	LED 1	LED 2
0	0	0	OFF	OFF
0	0	1	**ON**	**ON**
0	1	0	OFF	ON
0	1	1	ON	OFF
1	0	0	ON	OFF
1	0	1	OFF	ON
1	1	0	**ON**	**ON**
1	1	1	OFF	OFF